Field Support Manual
Central Processor Unit (P857EB)
P854
PTS6925

Data
Systems

PHILIPS

A PUBLICATION OF
PHILIPS DATA SYSTEMS
APELDOORN, THE NETHERLANDS

PUB. NO. 5122 991 30203

DATE August 1983

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SERVICE MANUAL STATUS RECORD

TITLE : CENTRAL PROCESSOR UNIT (P857EB)

PUBLICATION NUMBER : 5122 991 2971X

PUB. NO. 12TH DIGIT	UPDATE PACKAGE	SI. NO.	PAGES AFFECTED	DATE	REMARKS
1				8103	First Issue P857/A
2			All	8208	Update-P857EB
3		Up to P854-33	1-5/8, 1-18 thr. 1-21 1-23/25/31 2-5/7/13/14, 2-18/28/29/31 2-32/35, 3-6/12/14/15 3-17/18/24/26 3-28/30/33/35 3-36/40/49/53 3-55/58/59/62 3-65/68/69/77 3-81/82/84/89 3-90/95/110 3-113 thr. 3-134 3-140/143/144 3-147/151/152 4-5/12/17/19 4-21/31/33/37 6-2 thr.6-15	8308	Update-P857EB

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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

The P857E Micro-minicomputer is a general purpose digital computer suitable for scientific and industrial applications. A member of the P800 family the P857E combines the powerful programming advantages of the P857M with the smaller physical size of the Eurocard. The P857E employs Microprocessor technology to perform 3 CPU functions:

. Arithmetic Logic Unit, in the format of 4 x 4-bit slices to form the 16-bit word.
. Memory Address Sequensor, in the format of 4 x 4-bit slices to form the 16-bit memory address.
. Micro-Program Sequensor which has control over most CPU functions and their execution.

The P857E uses the P857 instruction set plus an extra three groups:

. Bit String Handling.
. Address Loading.
. Character String Handling.

The system input/output and control is with the Unified Product Line (UPL) Bus which interconnects all system units. The P857E may be connected with other devices in the P800 family via the UPL Bus; these devices are:

. GPBS (P851) Control Units.
. UPL Control Units and Memories.
. GPB (P856 and P857) Control Units using the Translator Card (TUGP).

The principle facilities available with the P857E are as follows:

. 16 hardware registers.
. V24 interface for operators peripheral.
. V24 interface for Control Panel.
. Power Failure/ Automatic Restart.
. Battery Back-Up after Power Failure.
. Real Time Clock.
. 2 IOP Channels (16 sub-channels).
. 32 parallel interrupts of which 4 are internal to the CPU.
. Up to 61 serial encoded interrupts.
. Hardware Bootstrap Loading with facility to load from one of 16 external devices.
. One of two serial Control Panels: HHCP - displays a hexadecimal address or data, FRCP - displays hexadecimal address and data simultaneously.
. Logical addressing for up to 32k, 16 bits (CPU function).
. Physical addressing for up to 8M words, 24 bits (MMU Function).
. Memory Protection on a Page basis (MMU Function).
. Stop On Preset Address for up to 1M word, 20 bits (SOPA Function)

The principle components showing their connection to the P857E are shown in Figure 1.1.

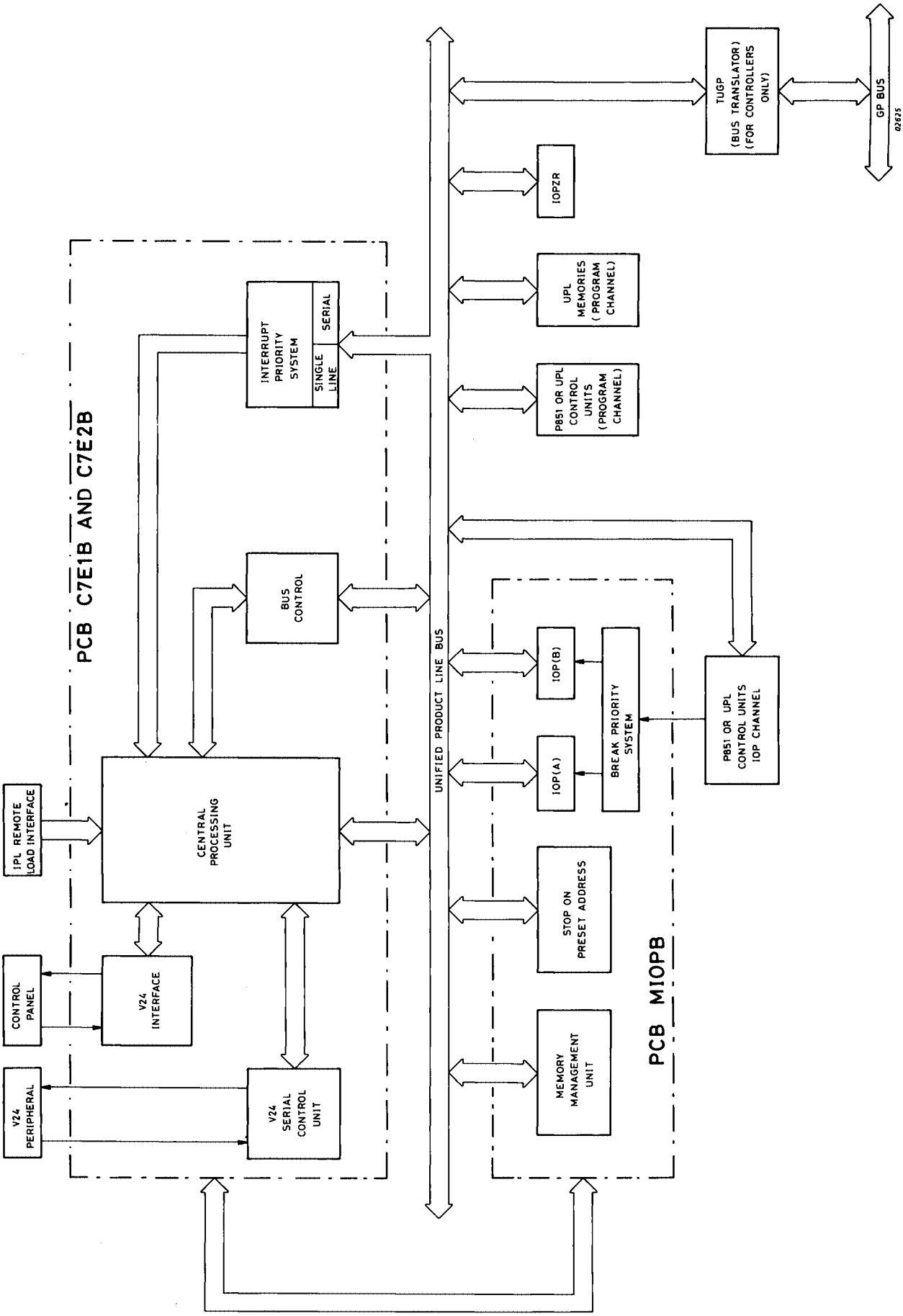


Figure 1.1 P857EB MAIN SYSTEM COMPONENTS

1.2 PHYSICAL DESCRIPTION

The P857E system cards (C7E2B, C7E1B and MIOPB) are all constructed on a Eurocard format, see paragraph 1.2.1.

1.2.1 SYSTEM EUROCARDS

All Eurocards (CPU, MIOP, Memories and some Control Units) are to the double

Eurocard format with two connectors:

. Connector 1 connects to the UPL Bus.
. Connector 2 is for special interconnections between cards.

One of the CPU cards (C7E2B) has 3 connectors fixed to the opposite end of the card:

. Connector 3 connects to the IPL Remote Load Interface.
. Connector 4 connects to the Control Panel Interface.
. Connector 5 connects to the V24 Peripheral Interface.

The Figure 1.2 shows the system of pinning and numbering of connectors for card C7E2. In general the same principle applies for all double Eurocards.

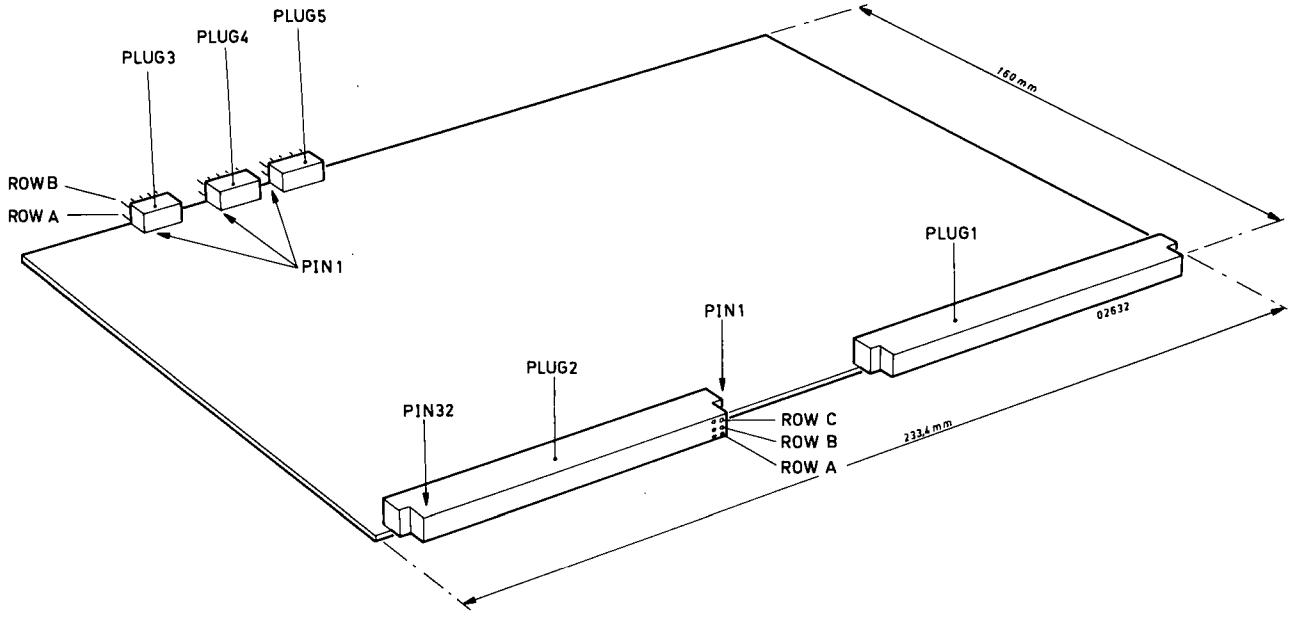


Figure 1.2 EUROCARD FORMAT (C7E2B)

Note: Note that the principle of numbering the connectors and their pin posi tions starts from Connector 1 pin 1 and continues in a clockwise direction around the card.

1.3 TECHNICAL DATA

The following description and tables are intended to give the user a reference to the P857E's performance, power requirements, physical characteristics and environmental conditions.

1.3.1 PERFORMANCE DATA

Central Processor Unit (Cards C7E1B and C7E2B).

. Cycle Time - 225nS, 270nS, 360Ns or Wait Cycle (270nS min. 11.5uS max.).
. Control Panel Interface 4.800 bits/sec.
. V24 Peripheral Interface, 16 combinations selectable by link between 50 to 19.200 bits/sec.
. Time-out signal releases the Bus after 11.5uS (Max.) due to an unsuccesful transfer.
. Real Time Clock: 20mS for 50 Hz.
16.66 mS for 60 Hz.
. Power Failure automatically initiated after 10mS.

Input Output Processor (Card MIOPB).

. One exchange - 1.7 uS (approx.) for input mode.
. Throughput exchanges 400 K words/sec. if the following conditions exist:

- memory access - 495nS (GMB1* in P851 Mode).
- memory release - 50nS
- C.U. access - 300nS
- C.U. release - 50nS

Memory Management Unit. (Card MIOPB)

. Translation time - 130nS (average) + memory access time.

* GMBI = UPL Memory.

1.3.2 POWER REQUIREMENTS

Table 1.1 shows the power requirements of C7E1B, C7E2B and MIOPB.

CARD	VOLTAGE	CURRENT	COMMENTS
C7E2B	+5VL	2.5A	
	+12VL	50mA	(without peripheral
	-12VL	30mA	devices connected)
C7E1B	+5VL	4A	
MIOPB	+5VL	2.6A	

Table 1.1 POWER REQUIREMENTS (C7E1B, C7E2B, MIOPB)

1.3.3 PHYSICAL CHARACTERISTICS

Table 1.2 shows the physical characteristics.

ITEM	NO.	DESCRIPTION
Eurorack	1	19 inch rack secured to cabinet at the front. Height of rack configurations, 6U or 12U.
Eurocards	12 or 22 max.	Size 160x233.4mm.
Component Mounting		The height of any component from the card surface must not exceed 10mm.
Eurorack Cover Plate	1	Suitable for rack configurations 6U or 12U high.
Control Panel	1	1 of control panels may be used - HHCP 78 mm. x 120mm., FRCP 180mm. x 130mm.
Control Panel Connection		Fixed or with a cable of 3 metres (max).
Eurorack Cable Support Plate	1	Fixed to the Eurorack for the routing of I/O cables to the back of the cabinet.

Table 1.2 PHYSICAL CHARACTERISTICS

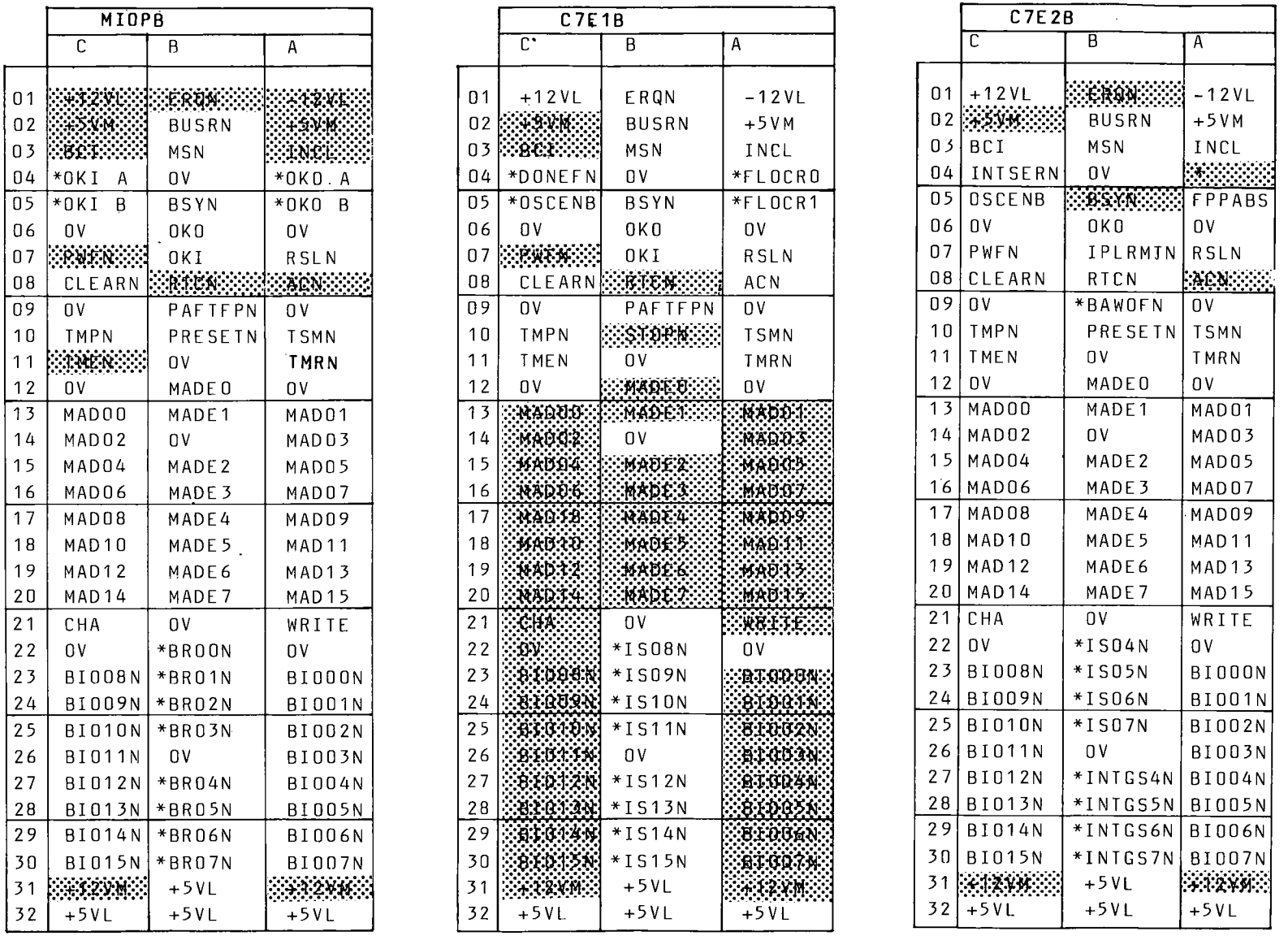
1.3.4 ENVIRONMENTAL CONDITIONS

t.b.f.

1.4 INTERFACES

This section lists all interface signals of the P857E. Figures 1.3 and 1.4 show a rear view of Connectors 1 and 2 and their corresponding signals. The Tables of 1.3 give the signal definitions in alphabetical order indicating the source and destination of the signals. The IPL Remote Load, Control Panel and V24 Peripheral Connectors are detailed in Tables 1.4, 1.5 and 1.6. A Test Connector for the connection of a test tool to Card C7E1B is given in Table 1.7. Note that Connectors 3, 4 and 5 are identical connectors so to prevent them being inserted in the wrong position the pins are keyed, see Tables 1.4, 1.5 and 1.6.

Note: The test tool is not a commercial product.



MIOPB

	C	B	A
01	+12VL	ERQN	-12VL
02	+5VM	BUSRN	+5VM
03	BCI	MSN	INCL
04	*OKI A	OV	*OKO A
05	*OKI B	BSYN	*OKO B
06	OV	OKO	OV
07	PWFN	OKI	RSLN
08	CLEARN	RTCN	ACN
09	OV	PAFTFPN	OV
10	TMPN	PRESETN	TSMN
11	TMEN	OV	TMRN
12	OV	MADE0	OV
13	MAD00	MADE1	MAD01
14	MAD02	OV	MAD03
15	MAD04	MADE2	MAD05
16	MAD06	MADE3	MAD07
17	MAD08	MADE4	MAD09
18	MAD10	MADE5	MAD11
19	MAD12	MADE6	MAD13
20	MAD14	MADE7	MAD15
21	CHA	OV	WRITE
22	OV	*BR00N	OV
23	BI008N	*BR01N	BI000N
24	BI009N	*BR02N	BI001N
25	BI010N	*BR03N	BI002N
26	BI011N	OV	BI003N
27	BI012N	*BR04N	BI004N
28	BI013N	*BR05N	BI005N
29	BI014N	*BR06N	BI006N
30	BI015N	*BR07N	BI007N
31	+12VM	+5VL	+12VM
32	+5VL	+5VL	+5VL

C7E1B

	C	B	A
01	+12VL	ERQN	-12VL
02	+5VM	BUSRN	+5VM
03	BCI	MSN	INCL
04	*DONEFN	OV	*FLOCR0
05	*OSCENB	BSYN	*FLOCR1
06	OV	OKO	OV
07	PWFN	OKI	RSLN
08	CLEARN	RTCN	ACN
09	OV	PAFTFPN	OV
10	TMPN	STOPN	TSMN
11	TMEN	OV	TMRN
12	OV	MADE0	OV
13	MAD00	MADE1	MAD01
14	MAD02	OV	MAD03
15	MAD04	MADE2	MAD05
16	MAD06	MADE3	MAD07
17	MAD08	MADE4	MAD09
18	MAD10	MADE5	MAD11
19	MAD12	MADE6	MAD13
20	MAD14	MADE7	MAD15
21	CHA	OV	WRITE
22	OV	*IS08N	OV
23	BI008N	*IS09N	BI000N
24	BI009N	*IS10N	BI001N
25	BI010N	*IS11N	BI002N
26	BI011N	OV	BI003N
27	BI012N	*IS12N	BI004N
28	BI013N	*IS13N	BI005N
29	BI014N	*IS14N	BI006N
30	BI015N	*IS15N	BI007N
31	+12VM	+5VL	+12VM
32	+5VL	+5VL	+5VL

C7E2B

	C	B	A
01	+12VL	ERQN	-12VL
02	+5VM	BUSRN	+5VM
03	BCI	MSN	INCL
04	INTSERN	OV	*
05	OSCENB	BSYN	FPPABS
06	OV	OKO	OV
07	PWFN	IPLRMIN	RSLN
08	CLEARN	RTCN	ACN
09	OV	*BAWOFN	OV
10	TMPN	PRESETN	TSMN
11	TMEN	OV	TMRN
12	OV	MADE0	OV
13	MAD00	MADE1	MAD01
14	MAD02	OV	MAD03
15	MAD04	MADE2	MAD05
16	MAD06	MADE3	MAD07
17	MAD08	MADE4	MAD09
18	MAD10	MADE5	MAD11
19	MAD12	MADE6	MAD13
20	MAD14	MADE7	MAD15
21	CHA	OV	WRITE
22	OV	*IS04N	OV
23	BI008N	*IS05N	BI000N
24	BI009N	*IS06N	BI001N
25	BI010N	*IS07N	BI002N
26	BI011N	OV	BI003N
27	BI012N	*INTGS4N	BI004N
28	BI013N	*INTGS5N	BI005N
29	BI014N	*INTGS6N	BI006N
30	BI015N	*INTGS7N	BI007N
31	+12VM	+5VL	+12VM
32	+5VL	+5VL	+5VL

Figure 1.3 CONNECTOR 1 LEVEL - C7E2B, C7E1B, MIOPB

** See SI P854-M-002 (only MIOPB)

	MIOPB		
	C	B	A
01	APN	BR08N	OSC
02	GPRESETN	BR09N	MADS00
03	BSYCPUEXN	BR10N	MADS01
04	BSYCPUN	BR11N	MADS02
05	TMRENB	BR12N	MADS03
06		BR13N	OV
07	OV	BR14N	ALU10
08	D00	BR15N	ALU11
09	D01	ALU04	ALU12
10	D02	PRESETN	ALU13
11	D03		ALU14
12	D04		ALU15
13	D05	ALUCIN	
14	D06	IS16N	SELR2
15	D07	IS17N	OKMMU
16	D08	IS18N.	FLAGCW3N
17	D09	IS19N.	BIORECN
18	D10	IS20N	PAFN
19	D11	IS21N	SELSPBUFN
20	D12	IS22N	
21	D13	IS23N	IEC3
22	D14	IS24N	IEC4
23	D15	IS25N	IEC5
24	ENBIOP	IS26N	INTGS2N
25	FUN	IS27N	INTGS3N
26	IOPN	OV	GPSPN
27		IS28N	INTE3N
28		IS29N	INTE1N
29		IS30N	RUNN
30	+5V * *	IS31N	GFETCH
31		BSYCN	WAIT
32	WRITEM		M10PABS

Figure 1.4 CONNECTOR 2 LEVEL - C7E2B, C7E1B, MIOPB

	C7E1B		
	C	B	A
01	APN	DONEFCPN	GPCHAN
02	GPRESETN	GPLRLDN	
03	BSYCPUEXN	ALU00	GPMADN
04	BSYCPUN	ALU01	SELIPLN
05	TMRENB	ALU02	TMFN
06	FPFABS	ALU03	IRUNA
07	FEN	ALU04	ALU10
08	D00	ALU05	ALU11
09	D01	ALU06	ALU12
10	D02	ALU07	ALU13
11	D03	ALU08	ALU14
12	D04	ALU09	ALU15
13	D05	ALUCIN	PUPF
14	D06	ALUI1	SELR2
15	D07	ALUI7	OKMMU
16	D08	ALUMADP1	GROUND (Back Panel)
17	D09	CR0	FLOACT
18	D10	CR1	PAFN
19	D11	NAD03	SELSPBUFN
20	D12		RUNIRN
21	D13	NAD08	IEC3
22	D14	NAD09	IEC4
23	D15	NAD10	IEC5
24	ENBIOP	SELCONSIN	INTEON
25	FUN	BSYCN	GPSPN
26	PCI3	DENB	INTGS1N
27	PCI2	BOFFN	SEL8251N
28	PCI1	TIMEOUT	INTE1N
29	PCI0	TMRZON	MIOPABS
30	PCCI	SELD2	GFETCH
31	LOADSN	SELD1	SEQCPU1
32	WRITEM	SELD0	SEQCPU0

	C7E2B		
	C	B	A
01	APN	DONEFCPN	OSC
02	GPCHAN	GPLRLDN	MADS00
03	BYSCPUEXN	ALU00	MADS01
04	BSYCPUN	ALU01	MADS02
05	GPMADN	ALU02	MADS03
06	OV	ALU03	IRUNA
07	FEN	ALU04	ALU10
08	D00	ALU05	ALU11
09	D01	ALU06	ALU12
10	D02	ALU07	ALU13
11	D03	ALU08	ALU14
12	D04	ALU09	ALU15
13	D05	ALUCIN	PUPF
14	D06	ALUI1	SELIPLN
15	D07	ALUI7	OKMMU
16	D08	ALUMAIP1	FLAGCW3N
17	D09	CR0	BIORECN
18	D10	CR1	PAFN
19	D11	NAD03	SELSPBUFN
20	D12	IOPN	RUNIRN
21	D13	NAD08	IEC3
22	D14	NAD09	IEC4
23	D15	NAD10	IEC5
24	ENB10P	SELCONSIN	INTGS2N
25	FUN	SELQTEN	INTGS3N
26	PCI3	DENB	INTGS1N
27	PCI2	BOFFN	INTEON
28	PCI1	TIMEOUT	SEL8251N
29	PCI0	TMRZON	RUNN
30	PCCI	SELD2	WAIT
31	LOADSN	SELD1	SEQCPU1
32	WRITEM	SELD0	SEQCPU0

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
ALU 00-15	C7E1/A * (2B03-12 2A07-12)	C7E2/A (2B03-12 2A07-12)	The output of the Arithmetic Logic Units which forms a 3-state connection to the ALU-BUS for output to BIO (C7E2/A) and interconnection of CPU functional units and the serial interfaces.
ALU 10-15	C7E1/A (2A07-12)	MIOP/C (2A07-12)	As above but routed to the MIOP to load the Scratch-Pad address Lines during WER and RER operation (IOP function) or TL, TS operations (MMU Function), PACC, PWR, RPA (PRESET Function).
ALU 04	C7E1/A	MIOP/B	Active low to specify a Preset Write operation (Stop on Preset Address function).
ALUCIN	C7E1/C (2B13)	C7E2/D,MIOP/G (2B13) (2B13)	A Microprogram signal for Arithmetic operations. It is also used for C7E2/D Interrupt Logic = 0 ALU PLR, = 1 IEC PLR and resets PWF F/F, and RTC F/F for MIOP/G to select ALU+1 mode.
ALUI1	C7E1/C (2B14)	C7E2/B (2B14)	For ALU operations this is a Microprogram signal used during multiply routines, and for loading an address (see signal ALUMADP1
ALUI7	C7E1/C (2B15)	C7E2/B (2B15)	For ALU operations this is a Microprogram signal to specify either a Shift Left (ALUI7 = 0) or a shift right (ALUI7 = 1).
ALUMADP1	C7E1/A (2B16)	C7E2/B (2B16)	For loading an address this signal is active in conjunction with ALUI1 to enable the incrementing of the Counter (type S169).
APN	C7E2 (2C01)	C7E1/D (2C01)	Indicates to the functional units that the CPU has begun a new cycle, and is the basic clock pulse that strobes the Micro-instruction Word and all data paths.
BAWOFN	Power Supply	C7E2/F (1B09)	When semi-conductor memories are employed, this signal (Battery Was Off) indicates that data has been lost.
BCI	UPL CU.s	C7E2/C (1C03)	A binary coded interrupt received in a serial format.
BIO 00-15N	C7E2/A (1A23-30 1C23-30)	MIOP/G (1A23-30 1C23-30)	Bidirectional data lines between C7E2/A. MIOP/G and all UPL Master and Slave units.

* Note: C7E1/A means C7E1B /diagram A

Table 1.3 INTERFACE SIGNALS

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
BIORECN	C7E2/F (2A17)	C7E1/E,MIOP/G (2A17) (2A17)	For a Read Cycle, this signal is enabled by APN and SEQWAIT of the previous cycle in order to read BIO.
BOFFN	C7E1/C (2B27)	C7E2/A (2B27)	The Microprogram ROMs enable BOFFN active low to inhibit the BIO Lines enabling an external FPP to set BIO.
BR00-07N	IOP C.U.s.	MIOP/A (2B01-08)	Break Request Lines (BR00 has highest priority).
BR08-15	IOP C.U.s.	MIOP/A (1B22-25,27-30)	Break Request Line (BR15 has lowest priority).
BSYCPUEXN	C7E1/E (2C03)	C7E2/B,MIOP/G (2C03) (2C03)	Active low indicates that the system executes a Translation (MMU function), during EL, ES instruction in System mode, or always in User mode.
BSYCPUN	C7E1/E (2C04)	C7E2/F,MIOP/C (2C04) (2C04)	Active low indicates that the CPU is busy with the Bus.
BSYCN	C7E1/E (2B25)	MIOP/G (2B31)	Indicates that the CPU is busy with the Bus. (= 0).
BSYN	UPL Masters	C7E1/E,MIOP/F (1B05) (1B05)	A bidirectional line between all UPL Masters; when a Master has been selected this line is low to indicate BuSY (Bus Occupation) to other Masters.
BUSRN	UPL Masters	C7E2/F(1B02) C7E1/E(1B02) MIOP/G(1B02)	A bidirectional line between all UPL Masters; any Master may force this line low to request the Bus.
CHA	C7E2/B(1C21) MIOP/D(1C21)	UPL Bus	When received by the memory CHA = 1 for Character operation and CHA = 0 for Word operation. For Control Units and External Registers CHA = 0.
CLEARN	C7E2/A (1C08)	C7E1/E(1C08) MIOP/F(1C08)	General reset of all devices active low for a minimum time of 10uS
CR0,CR1	C7E1/D (2B17,18)	C7E2/D (2B17,18)	Contents of the Condition Register form a part of the P.S.W.
DENB	C7E2/F (2B26)	C7E1/E (2B26)	The CPU has requested the Bus (Demand Exchange Enable), so DENB sets the BSYCPU F/F and at the end of a WRITE cycle this inhibits the setting of BSYCPU, if TSM is still active.

Table 1.3 INTERFACE SIGNALS (CONTD.)

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
D00-15	C7E2/A (2C08-28)	C7E1/B,MIOP/D (2C08-23)	Internal tri-state D-BUS interconnecting the functional units on C7E1, C7E2 and the MIOP card.
DONEFCPN	C7E1/E (2B01)	C7E2/F (2B01)	After a transfer with the FPP this signal restarts the CPU Sequensor which is in a WAIT cycle.
DONEFN	FPP	C7E1/E (1C04)	Indicates to the CPU that the FPP has finished the transfer.
ENBIOP	C7E1/C (2C24)	C7E2/F,MIOP/G (2C24) (2C24)	For IOP transfers this Microprogram signal enables the IOP. It holds the CPU Sequensor in the WAIT cycle until IOP has finished a transfer of data.
ERQN	C71/E (1B01)	UPL MASTERS	To prevent a Master from activating his BUSRN Signal.
FEN	C7E2/D (2C07)	C7E1/E (2C07)	Bit 13 of the P.S.W. it must always be "0" for RTN A15.
FLAGCW3N	MIOP/E (2A16)	C7E2/F (2A16)	A Flag sent to the CPU to indicate the IOP has received the 2nd Control Word and that the next WER is for the 3rd control word.
FLOACT	C7E1/D (2A17)	FPP	Sent at the beginning of an FFX instruction to time the actual processing and to synchronise the end of the operation.
FLOCRO,CR1	FPP	C7E1/D (1A04,05)	From the FPP Condition Register to indicate the result of an operation which is then taken into account by the CPU Condition Reg.
FPPABS	FPP	C7E2/F (1A05)	When the FPP card is inserted this signal is forced low.
FUN	C7E2/D (2C25)	C7E1/E,MIOP/G (2C25) (2C25)	Indicates User Mode (= 1) and System Mode (= 0).
GFETCH	C7E1/C (2A30)	MIOP/B (2A30)	Indicates an instruction Fetch cycle and restarts CPU sequensor in some cases.
GPCHAN	C7E1/C (2A01)	C7E2/C (2C02)	A Microprogram signal to indicate Character operation, this signal has the meaning as CHA (already described) Also to clock ALUX reg. and force RUN.

Table 1.3 INTERFACE SIGNALS (CONTD.)

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
GPLRLDN	C7E1/C (2B02)	C7E2/D (2B02)	A Microprogram signal to load the Program Level Register.
GPMADN	C7E1/C (2A03)	C7E2/B (2C05)	A Microprogram signal to enable the loading or incrementing of the MADSE 7,6,5,4 Buffer.
GPRESETN	C7E1/C (2C02)	MIOP/D (2C02)	A Microprogram signal to reset the Preset Address Buffer (Stop on Preset Address function), or to load this buffer.
GPSPN	C7E1/C (2A25)	MIOP/G (2A26)	A Microprogram signal to enable the access of the MIOP Scratch Pad.
IEC 3,4,5	C7E1/D MIOP/A (2A21,22,23	C7E2/C (2A21,22,23)	A 3-bit code encoded from the parallel interrupts 08-15N.
INTGS1N	C7E1/D (2A26)	C7E2/C (2A26)	An output from interrupts 08-15N which is used to generate the IEC 0, 1,2 Lines.
INTGS2N	MIOP/A (2A24)	C7E2/C (2A24)	An output from interrupts 16-23N which is used to generate the IEC 0, 1,2 Lines.
INTGS3N	MIOP/A (2A25)	C7E2/C (2A25)	An output from interrupts 24-31N which is used to generate the IEC 0, 1,2,3 Lines.
INTS4-7N		C7E2/C (1B27-30)	Spare positions available for extending the Interrupt System.
INTEON	C7E2/C (2A27)	C7E1/D (2A24)	Enable interrupts IS8-15.
INTE1N	C7E1/D (2A28)	MIOP/A (2A28)	Enable interrupts IS16-23
INTE3N	MIOP/A (2A27)	--	Spare position available for extending the Interrupt System from 31 onwards.
INCL	C7E2/C (1A03)	UPL CUs	The serial INterrupt Clock generated by the CPU to synchronise interrupt code from the CUs. The frequency is not constant and depends on the CPU cycle.
IRUNA	C7E2/C (2A06)	C7E1/C (2A06)	An input to the Microprogram Sequensor Test Logic to indicate that either an Interrupt or RUN condition is active.

Table 1.3 INTERFACE SIGNALS (CONTD.)

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
IPLRMTN	Remote Terminal	C7E2/F (1B07)	Indicates to the CPU External Test logic that a code is to be received on Lines OPS 00N-03N.
INTSERN	C7E2/A (1C04)	IS Lines	An interrupt from the Operator Interface (SERial INTerface) when either a Write, Read, Wait State, Echo condition is active.
IOPN	MIOP/F (2C26)	C7E2/F (2B20)	Indicates to the CPU that the IOP has either requested or is busy with the Bus
IS04-07N	CUs	C7E2/C (1B22-25)	Interrupt Request Lines Group 1.
IS08-15N	CUs	C7E1/D (1B22-30)	Interrupt Request Lines Group 2.
IS16-31N	CUs	MIOP/A (2B14-25,27-30)	Interrupt Request Lines Group 3.
LOADSN	C7E1/C (2C31)	C7E2/B (2C31)	A Microprogram signal to enable the loading of the MADS 00-15 Buffer.
MAD 00-15	C7E2/B MIOP/D (1C13-20 1A13-20)	UPL	Used in with MADE0-7 to represent a memory address in true value; MADE 0 is the most significant and MAD15 the least significant bit.
MADS 00-03	C7E2/B (2A02-05)	MIOP/C (2A02/-05)	When the MMU is being used these lines contain a page address 00-15.
MADE 0-7	C7E2/B MIOP/D (1B12,13 15-20)	UPL Mems	See above (MAD 00-15)
MIOPABS	MIOP/G (2A32)	C7E1/E (2A29)	When the MIOP card is correctly inserted in the rack this signal is forced low.
MSN	UPL Masters	C7E2/F(1B03) C7E1/E(1B03) MIOP/G(1B03) (1B03)	A bidirectional line between all UPL Masters; originating from the Master selected to indicate to all other Masters that Master is selected.
NAD03	C7E1/B (2B19)	C7E2/A (2B19)	One of the Next Address Lines. Used to select V24- or CP interface
NAD08,09,10	C7E1/B (2B21-23)	C7E2/A (2B21-23)	The combination of these Next Address signals enables the reading or writing of data or control information at the serial interfaces.

Table 1.3 INTERFACE SIGNALS (CONTD.)

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
OKO	C7E2/F (1B06)	C7E1/E (1B07)	The Bus Controller sends OKO to search for the highest priority Master requesting the Bus. OKO is routed through card C7E1B to the next priority Master (which could be MIOP/G if fitted).
OKIA	C7E1/E (1B06)	MIOP/G (1C04)	Derived from the Bus Controller OKO signal, OKIA is the input to IOPA of the MIOP.
OKOA	MIOP/G	MIOP/G (1A04)	If IOPA was not the Master requesting the Bus then signal OKOA becomes an input to the next priority Master (e.g. IOPB, if connected).
OKIB	MIOP/G	MIOP/G (1C05)	Continuing the OKO chain, signal OKIB is the input to IOPB of the MIOP.
OKOB	MIOP/G	MIOP/G (1A05)	If IOPB was not the Master requesting the Bus then signal OKOB becomes an input to the next priority Master.
OKMMU	MIOP/G	C7E1/E(2A15) C7E2/D(2A15)	If no Page Fault, OKMMU = 1 indicates that MAD is loaded. BSYCPUEXN resets it for the next Translate cycle.
OSC	C7E2/E (2A01)	MIOP/F (2A01)	Derived from the CPU basic clock frequency this signal forms the basic 45nS pulse for the MIOP card functions.
OPSON-3N	Remote Device	C7E2/F (3A01,02 3B01,02)	Four address lines, the code of which is used to address the last sixteen words of the Bootstrap.
OSCENB	C7E1/D (1C05)	C7E2/E (1C05)	A test input from the Development Test Tool to enable or inhibit the CPU clock pulse.
PAFN	MIOP/G (2A18)	C7E2/F(2A18) C7E1/E(2A18)	The CPU is in a WAIT cycle but due to Page Fault Detection there is no TMRN or TSMN, so this signal restarts the CPU Sequensor.
PAFTFPN	MIOP/C (1B09)	C7E1/C (1B09)	A test condition to indicate to the Microprogram Sequensor (2910) that either a Page Fault has occured (active low) or not (high).
PCI 0-3	C7E1/C (2C26-29)	C7E2/B (2C26-29)	A code from the Microprogram defining micro-instruction that must be executed by the Address Sequensor.

Table 1.3 INTERFACE SIGNALS (CONTD.)

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
PCCI	C7E1/C (2C30)	C7E2/B (2C30)	A signal from the Microprogram which is the Carry Input for the Address Sequensor
PRESETN	MIOP/B (1B10)	C7E2/C (1B10)	Indicates that a Preset Address is found (Stop on Preset Address function).
PUPF	C7E2/C (2A13)	C7E1/B (2A13)	Indicates that either Control Panel or Remote Device wants to send a code or that the Preset Address is found.
PWFN	Power Supply	C7E2/D (1C07)	Indicates to the CPU that a Power Failure has occurred.
RSLN	Power Supply	C7E2/A(1A07) C7E1/E(1A07) MIOP/F(1A07)	To ensure an orderly start procedure this signal stays low until power has stabilised.
RTCN	Power Supply	C7E2/F (1B08)	Real Time Clock signal, derived from mains frequency (generated every 20mS for 50HZ mains frequency).
RUNIRN	C7E2/C (2A20)	C7E1/B (2A20)	For a RUN or InteRrupt or Control Panel condition this signal causes PLAMAP to enable an address on the NAD Lines which in turn enables the Micro-Routine start start address.
RUNN	C7E2/D (2A29)	MIOP/B (2A29)	After a stop on preset address this signal resets the Preset F/F as soon as the RUN bit in PSW is reset by microprogram.
SELD 0,1,2	C7E1/C (2B30-32)	C7E2/D (2B30-32)	A code from the Microprogram which enables the generation of the Bus D Emitter Selection signals for card C7E2. Also to select the Serial interfaces 8251.
SELR2	C7E1/C (2A14)	MIOP/G (2A14)	A Microprogram signal which when = 1 indicates that the General Purpose Register selected by the R2 field is used as a destination. Also to write new information in MIOP scratch pad and PRESET buffer or to set SPFLAG.
SELSPBUFN	C7E1/C (2A19)	MIOP/D(2A19) C7E2/D(2A19)	Enables the MIOP Scratch Pad Buffer content onto the D Bus (MIOP) and inhibits the selection of the Bus D emitters (C7E2).
SEQCPU0,1	C7E1/C (2A31,32)	C7E2/E (2A31,32)	A code from the Microprogram which selects the CPU cycle type at the CPU Sequensor.

Table 1.3 INTERFACE SIGNALS (CONTD.)

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
TMEN	C7E1/E (1C11)	C7E2/F(1C11) Ext. Regs.	Timing Master to External Register, active low to validate the addresses and data; this signal also resets the time-out circuit (C7E2).
TMPN	C7E1/E MIOP/F (1C10)	C7E2/F(1C10) C.U.s	Timing Master to Peripheral, active low to validate the addresses and data; this signal is also used to reset the Time-out circuit (C7E2).
TMRN	C7E1/E MIOP/F (1A11)	C7E2/F(1A11) Mems	Timing Master to RAM (or other memory types), active low to validate adresses and data; this signal also resets the Time-out circuit (C7E2).
TSMN	C.U.s	C7E2/F(1A10) C7E1/E(1A10) MIOP/F(1A10) UPL Masters	This signal is the reply to TMEN, TMPN or TMRN and is used to restart the CPU Sequensor which is in a WAIT cycle (C7E2), reset the BSYCPU F/F (C7E1) and restart the MIOP (MIOP).
TMFN	C7E1/C (2A05)	FPP	Timing Master to Floating Processor, active low to validate data.
TIMEOUT	C7E2/E (2B28)	C7E1/E (2B28)	Once an exchange is initiated the Time-out circuit starts counting and if the TSMN signal is not received within approx. 11uS then this signal (if CPU exchange) sets the CPU Condition Register, resynchronises the Master by generating TSMN.
TMRZON	C7E2/F (2B29)	C7E1/E (2B29)	At the end of an exchange (TSMN received) this signal reset the signals TMEN, TMPN, TMRN.
TMRENB	C7E1/C (2C05)	MIOP/B (2C05)	For the Stop on Preset Address function this signal ensures that the instruction is fetched before enabling PRESETN.
WAIT	C7E2/E (2A30)	MIOP/B (2A31)	For the Stop on Preset Address function when the address is found a Memory cycle is executed which means a CPU WAIT cycle and so signal WAIT is active to clock the PRESETA F/F (WAIT also resynchronises the CPU Sequensor
WRITE	C7E2/B MIOP/D (1A21)	UPL Bus	Indicates to the UPL Slaves the direction of Bus transfer; WRITE = 1 means transfer Master to Slave; WRITE = 0 means transfer Slave to Master.

Table 1.3 INTERFACE SIGNALS (CONTD.)

Signal Name	Source (Pin No.)	Destination (Pin No.)	Description
WRITE	C7E2/B MIOP/D (1A21)	UPL Bus	Indicates to the UPL Slaves the direction of Bus transfer; WRITE = 1 means transfer Master to Slave; WRITE = 0 means transfer Slave to Master.
WRITEM	C7E1/C (2C32)	MIOP/B(2C32) C7E2/A(2C32)	A Microprogram signal indicating a WRITE operation, the logic levels have the same value as WRITE (above). WRITEM is also used for several other purposes (chapter 3).

Table 1.3 INTERFACE SIGNALS (CONTD.)

C7E2B Pin No.	Signal Name	Description	Source	Destination
3B03	OPSON	Address Lines from a Remote Device to address the last 16 words of the Bootstrap Key position	Remote Device	C7E2/F
3B02	OPS1N			
3B04	OPS2N			
3B01	OPS3N			
3A05	not connected			
3A01-04	0V			
3B05	0V			

Table 1.4 IPL REMOTE LOAD INTERFACE - CONNECTOR 3

C7E2B Pin No.	Signal Name	Description	Source	Destination
4B01	LOCK	= 0 Control Panel functions are enabled. = 1 Control Panel functions (except INT) are inhibited.	FRCP	C7E2/A
4B03	0V			
4A01	SDPM	Serial Data (CT104)	FRCP	C7E2/A
4B02	SDMP	Serial Data (CT103)	C7E2/A	FRCP
4A02	RTCE	= 0 inhibit Real Time Clock = 1 enable Real Time Clock	FRCP	C7E2/F
4A03	RESETN	Master Reset	C7E2/A	FRCP
4B04	+5V			
4A04	-12V			
4A05	not connected	(key position)		
4B05	+12V			

Table 1.5 CONTROL PANEL INTERFACE (FRCP) - CONNECTOR 4

C7E2B	Signal Name	Description	Source	Destination
5B02	CT103	Serial Data	C7E2/A	D.T.E.
5A01	CT104	Serial Data	D.T.E.	C7E2/A
5A02	CT107	Modem Ready	D.T.E.	C7E2/A
5B03	CT108	Connect Modem to Line	C7E2/A	D.T.E.
5A03	CT133	Ready for Receiving	D.T.E.	CP7E2/A
5B01	0V			
5A04	0V			
5A05	0V			
5B04	0V			
5B05	not connected	key position		

Table 1.6 V24 PERIPHERAL INTERFACE - CONNECTOR 5

Pin	Signal Name	Description
3A01	ROMAD08	Microprogram ROM Address Lines, note that only 9 of the 11 lines are available here, for ROMAD09 and 10 see pins 3B17 and 3B18 (C7E1/B).
02	07	
03	06	
04	05	
05	04	
06	03	
07	02	
08	01	
09	ROMAD00	
10		
11	BSYCPU	Indicates CPU busy with Bus (C7E1/E).
12	TMPN	Indicates Transfer Master to Peripheral (C7E1/E).
13	TMRN	Indicates Transfer Master to Memory (C7E1/E).
14	OSCENB	Enables the internal clock (C7E1/D).
15		Not used
16		Not used
17	RSLAN	Simulates RSLN from the Power Supply (C7E1/E).
18	APTEST	Enables an external test of the CPU Sequensor signal AP (C7E1/D).
19	5V	
20	5V	
3B01	D00	3-state internal CPU Bus (C7E1/B).
02	01	
03	02	
04	03	
05	04	
06	05	
07	06	
08	07	
09	08	
10	09	
11	10	
12	11	
13	12	
14	13	
15	14	
16	D15	
17	ROMAD10	See pin nos. 3A01-3A09.
18	ROMAD09	See pin nos. 3A01-3A09.
19	0V	
20	0V	

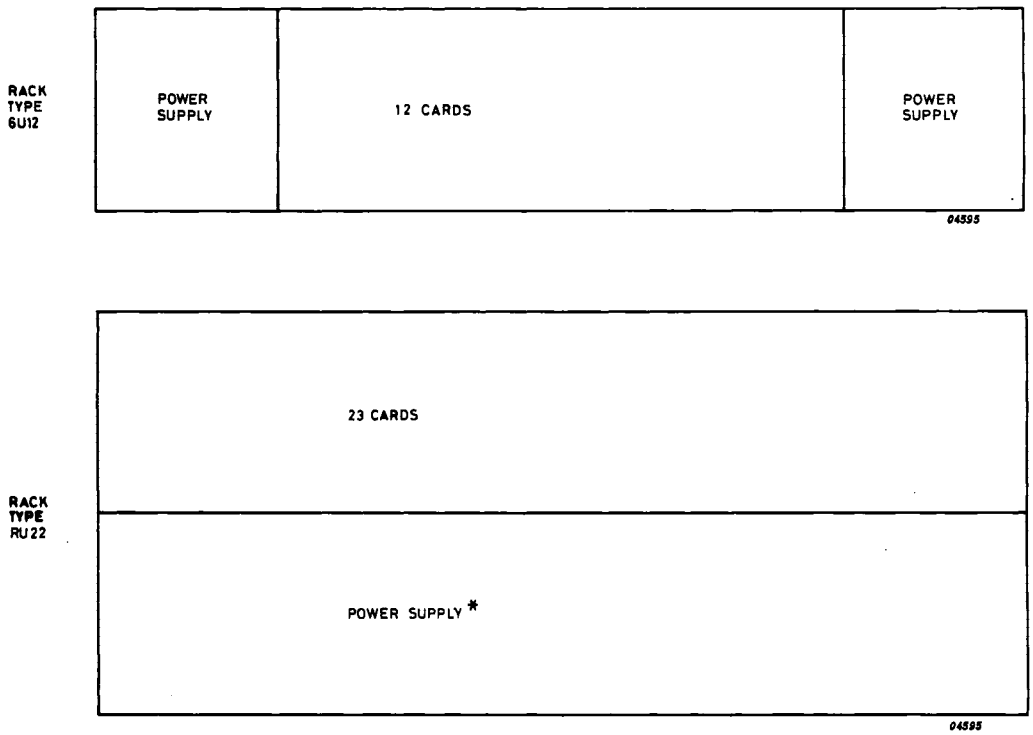
Table 1.7 TEST CONNECTOR FOR TESTTOOL ONLY (CARD C7E1B)

1.5 APPLICATION NOTES

The P857E system is housed in a Eurorack configuration which includes the UPL Bus, System Cards and Power Supply. Two rack configurations are possible (see figure 1.5).

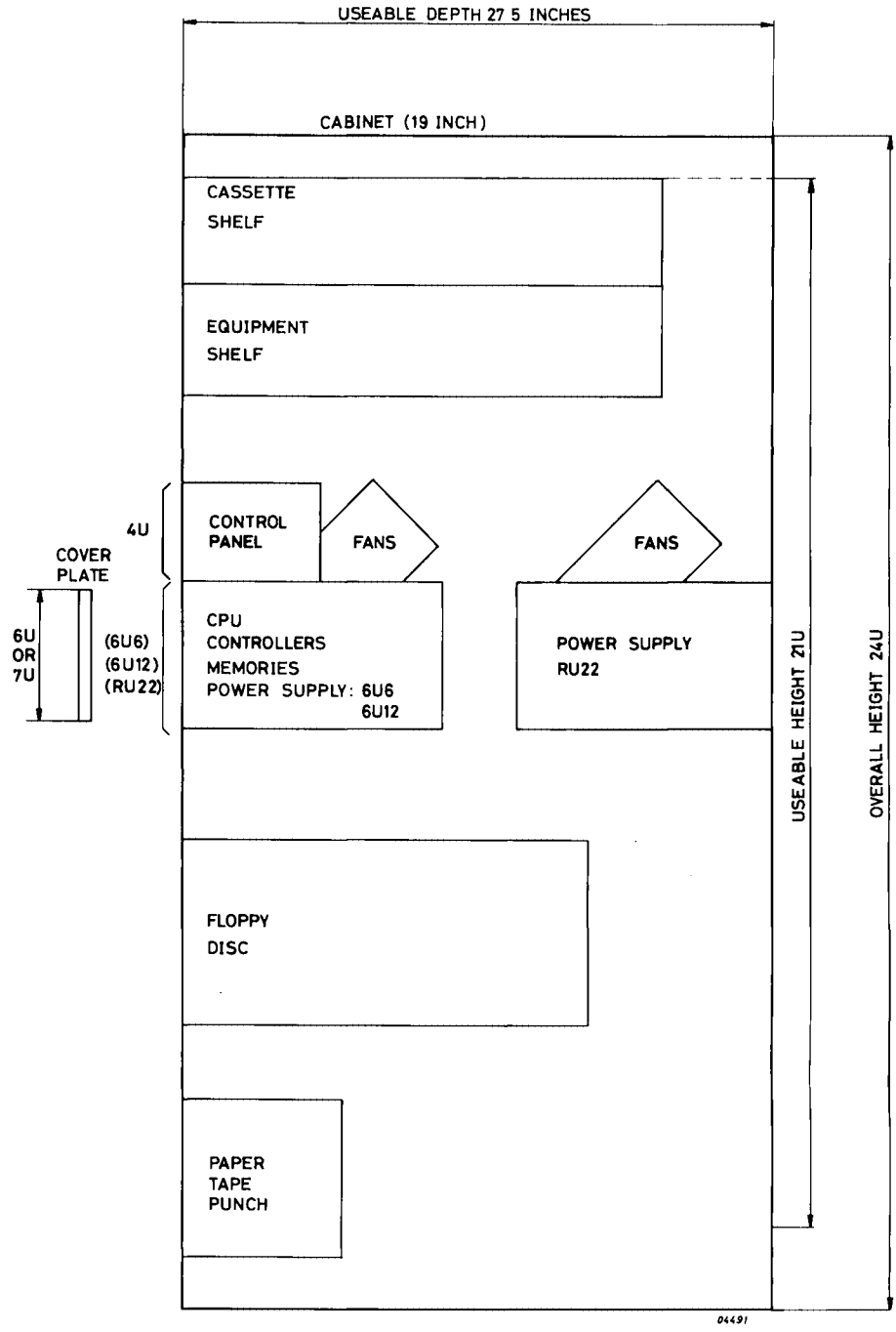
. 6U12 to contain 12 cards max.
. RU22 to contain 23 cards max.

These 2 Eurorack configurations may be housed in a cabinet, an example of which is shown in Figure 1.6. The UPL Bus must never be extended out of the CPU Rack without the signals being terminated with a Terminator Card.



* Power supply is placed on backside of cabinet opposite the Logic rack.

Figure 1.5 RACK CONFIGURATIONS



Notes: 1) 6U12 rack (P854-300): Control panel (if necessary) in 4U cover-plate
key-switch in 6U12 rack.
2) RU22 rack (P854) : Control panel and key-switch in 4U cover-plate
Fan assy's on logic- and power rack.

Figure 1.6 EXAMPLE OF A CABINET CONFIGURATION

1.5.1 CONFIGURATION RULES

When the P857E configuration is being assembled the following rules must be taken into account:

- Cards C7E2B, C7E1B and MIOPB must be in rack positions 1, 2 and 3 respectively.
- Other Masters follow in order of their system priority, determined by links OKO and OKI.
- Card MIOPB contains 2 IOPs; IOPA and IOPB. IOPA must always have a higher priority than IOPB (determined by links OKOA/B and OKIA/B).
- Control Unit addresses with MIOP present $\leqslant$ /F without MIOP any address may be used.
- The UPL Bus must not be extended out of the basic Eurorack without the signals being terminated.

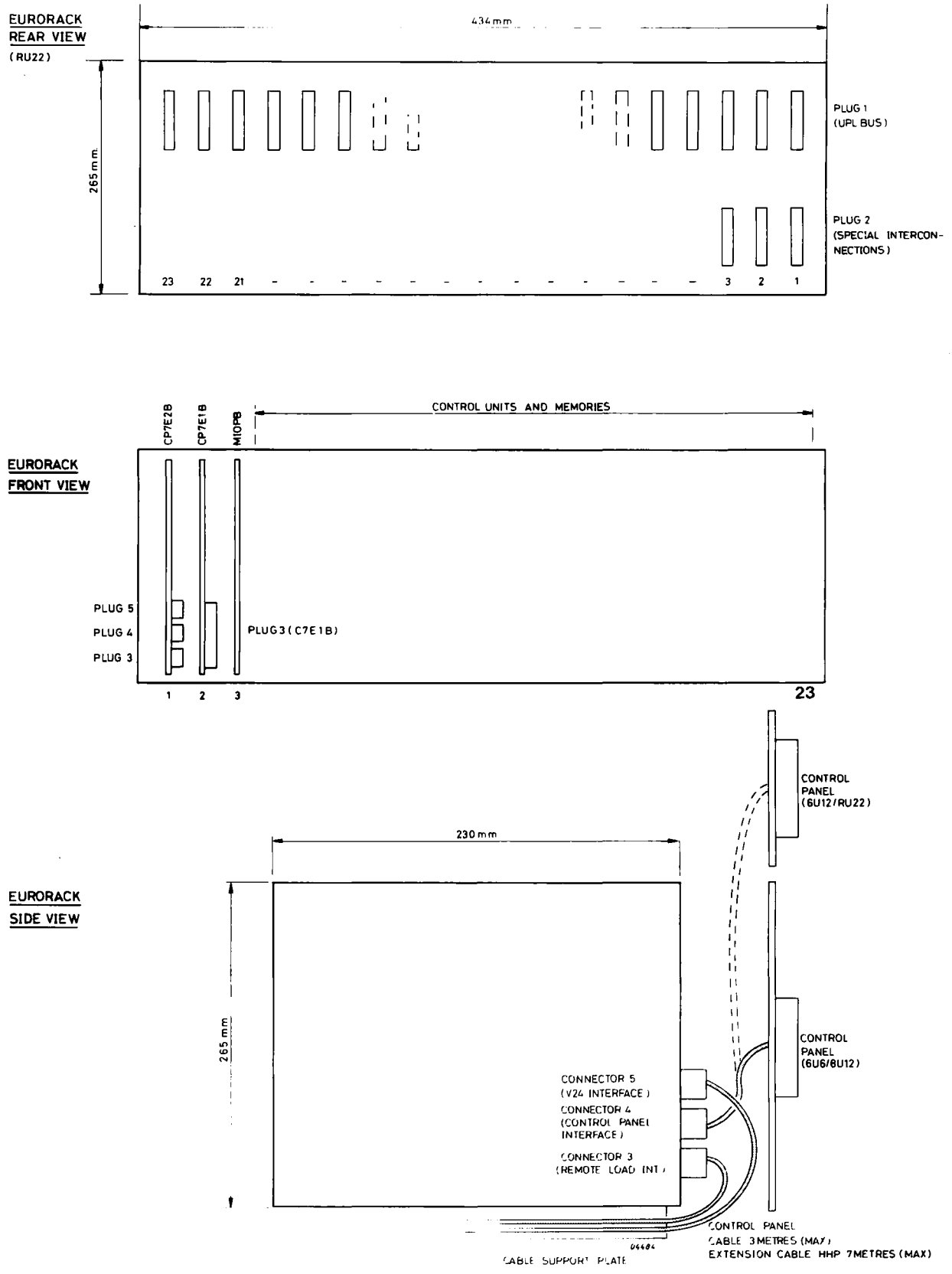
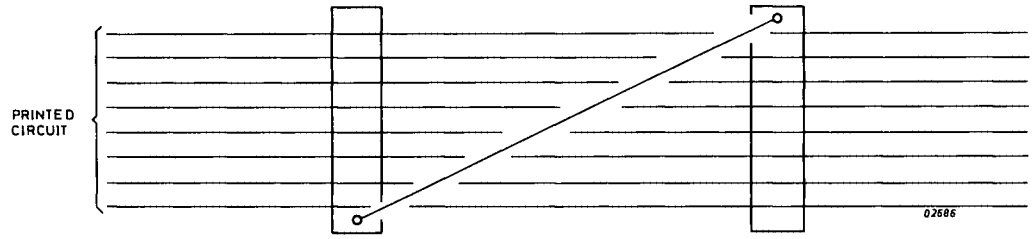


Figure 1.7 EURORACK

1.6 INSTALLATION DATA

The following instructions are only intended to highlight the important aspects of installing this system.

- Insert the Eurorack into the front of the cabinet and screw into position.
- Ensure that the mains are connected in accordance with the specification (this may differ depending upon the country of installation.
- Ensure that the Grounding Rules are observed.
- Check the card links before inserting cards into the Eurorack.
- Ensure that the cables between Control Units and Devices are firmly secured and that the screens of these cables are connected in accordance with the Grounding Rules.
- Interrupts and Breaks must be wired so that they run across the printed circuit and NOT parallel to it (see below).



WIRED CONNECTION RUNNING ACROSS THE PRINTED CIRCUIT

1.6.1 STRAP SETTINGS

There are straps fitted to all 3 cards but only C7E2B houses the straps that are selectable by the user.

- IPL links to select the IPL and program loading device for remote and/or auto IPL. (table 1.8)
- CT133 link.
- Speed Selection Links for the V24 peripheral interface (Table 1.9). All cards must be checked to ensure that the workshop test links are in position, see Figures 1.8, 1.9 and 1.10.

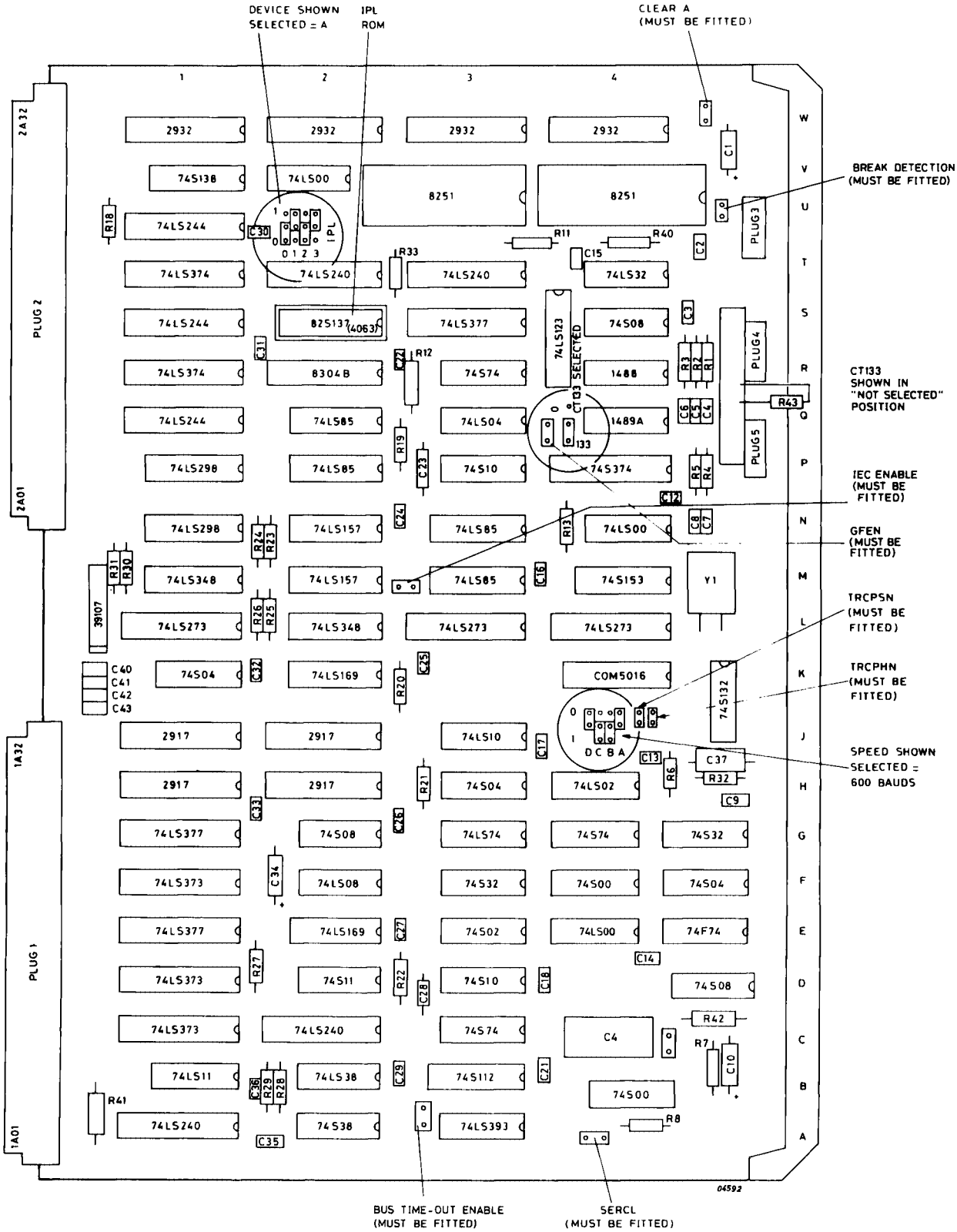


Figure 1.8 C7E2B COMPONENT LAYOUT AND LINKS

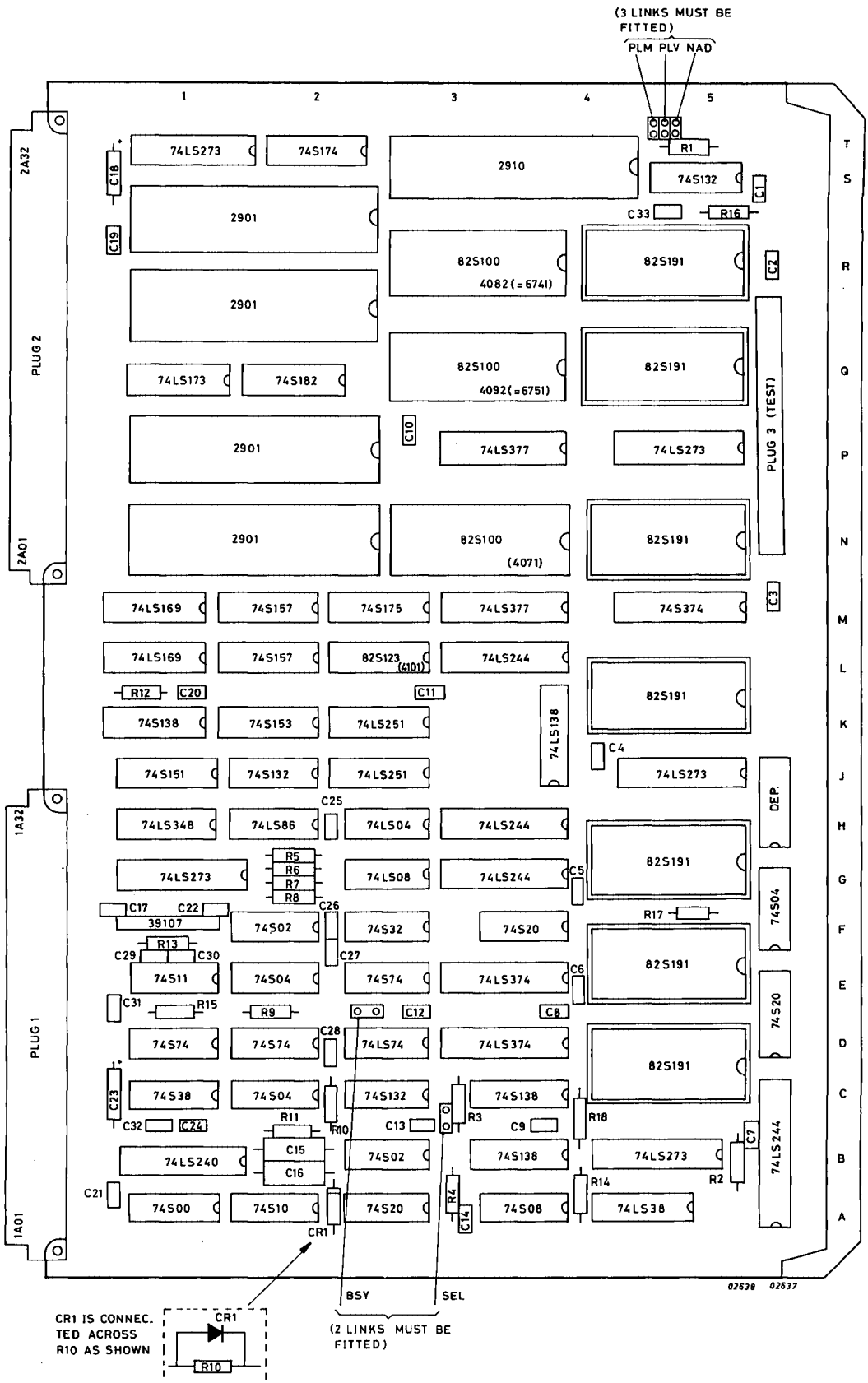


Figure 1.9 C7E1B COMPONENT LAYOUT AND LINKS

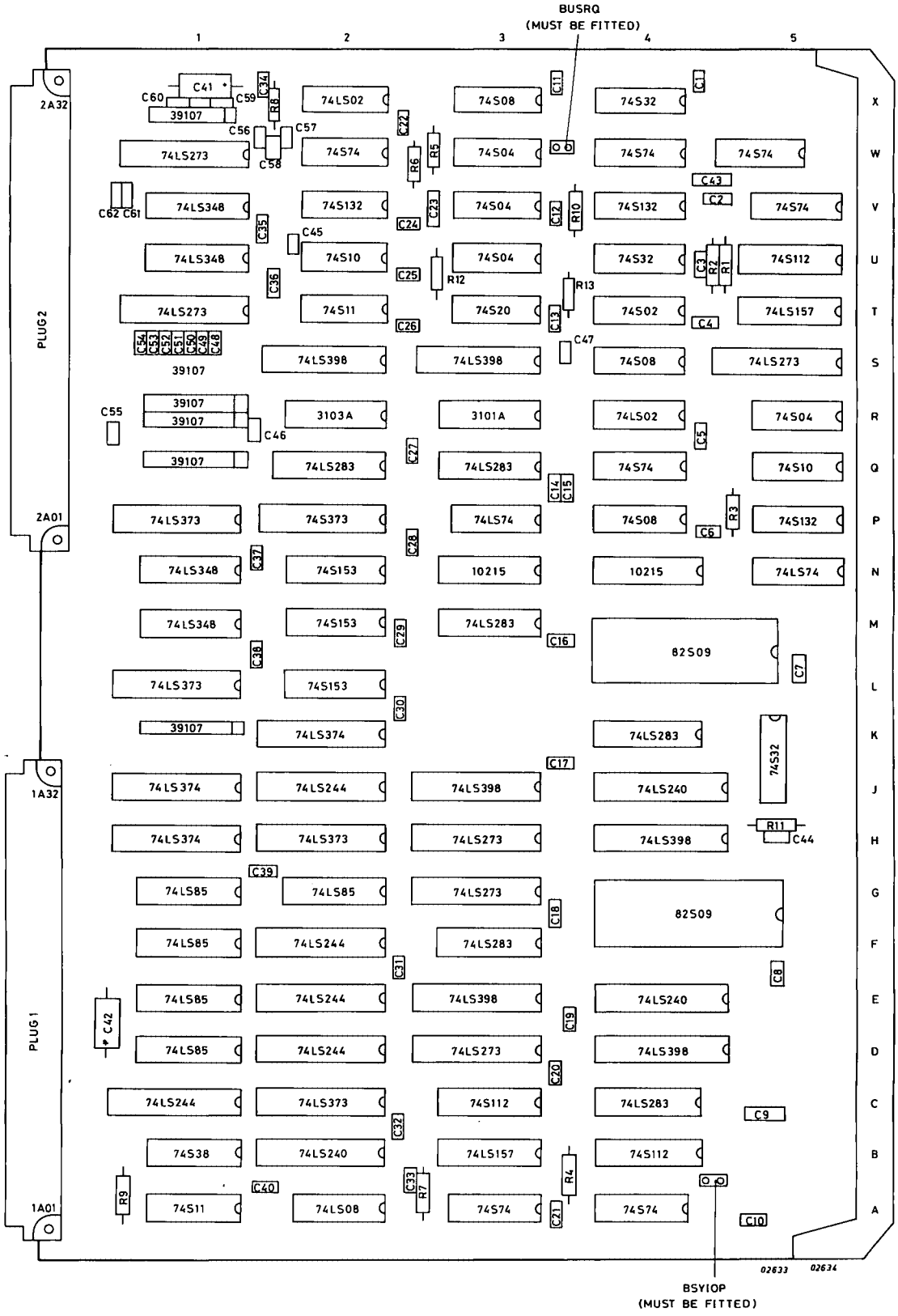
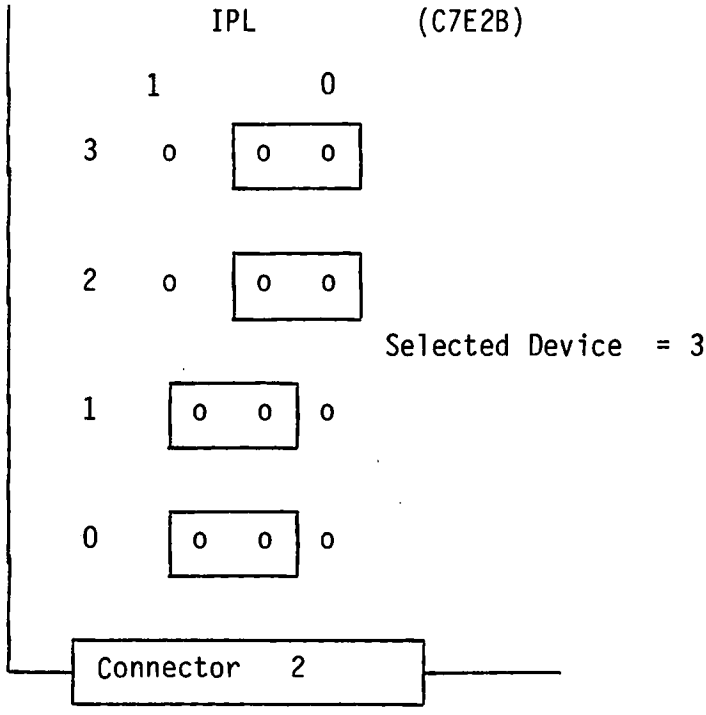


Figure 1.10 MIOPB LAY OUT AND LINKS

3	2	1	0		MEMORY ADDRESS
OPS3N	OPS2N	OPS1N	OPSON	WORD	HEX
0	0	0	0	0	1FE
0	0	0	1	1	1FC
0	0	1	0	2	1FA
0	0	1	1	3	1F8
0	1	0	0	4	1F6
0	1	0	1	5	1F4
0	1	1	0	6	1F2
0	1	1	1	7	1F0
1	0	0	0	8	1EE
1	0	0	1	9	1EC
1	0	1	0	10	1EA
1	0	1	1	11	1E8
1	1	0	0	12	1E6
1	1	0	1	13	1E4
1	1	1	0	14	1E2
1	1	1	1	15	1E0

Table 1.8 SELECT-IPL (REMOTE LOAD)

The following diagram shows the identification that is silkscreened on the card and an example of word selection.

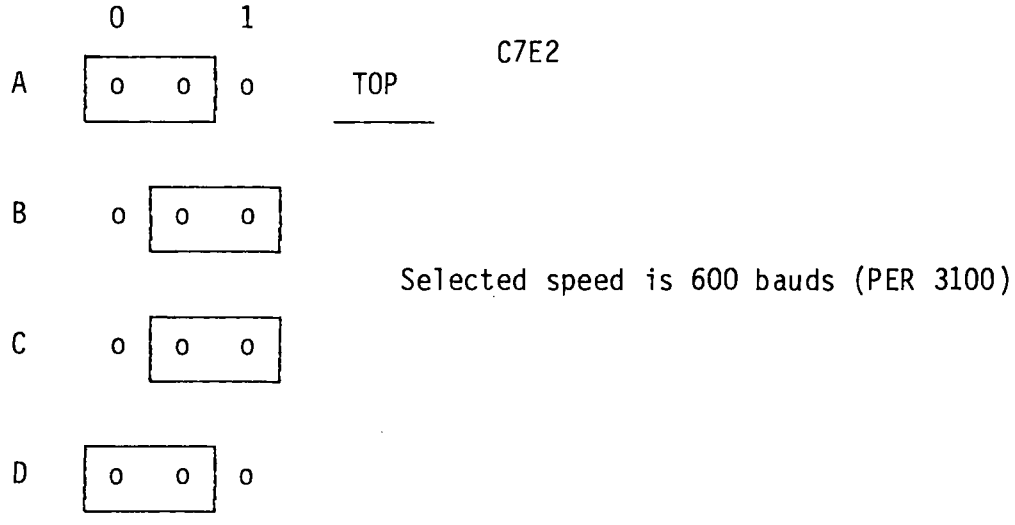


Transmit/Receive U Link Positions				Baud Rate
D	C	B	A	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134,5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1.200
1	0	0	0	1.800
1	0	0	1	2.000
1	0	1	0	2.400
1	0	1	1	3.600
1	1	0	0	4.800
1	1	0	1	7.200
1	1	1	0	9.600
1	1	1	1	19.200

shown

Table 1.9 V24 - PERIPHERAL INTERFACE - SPEED SELECTION

The following diagram shows an identification that is silkscreened on the card, and an example of speed selection:



1.6.2 MOUNTING

T.b.f.

The three cards C7E2B, C7E1B and MIOP must be mounted on dedicated positions 1,2 and 3 of the UPL rack (see figure 1.6).

1.6.3 INTERCONNECTIONS

System interconnections between the cards at the UPL Bus Connector level are as follows:

. Interrupts
. Breaks
. OKO/OKI Links

An example of these interconnections is given in Figure 1.11.

1.6.4 COMPATIBILITY

The P857E is compatible with other P800 systems in the following cases:

. P857 instruction set.
. UPL (Eurocard) Memories.
. Pin compatibility with P851 and UPL (Eurocard) Control Units.
. GPB Control Units using TUGP (Translator UPL/GPB Card).
. For P857M, the IOP Control Word 1 (WER1) loaded MAD64 and MAD128 (bits 2 and 3 respectively). For P857E this is still respected but if WER3 is used then these bits MAD128 and MAD64 (MADE6 and MADE7) are overwritten.

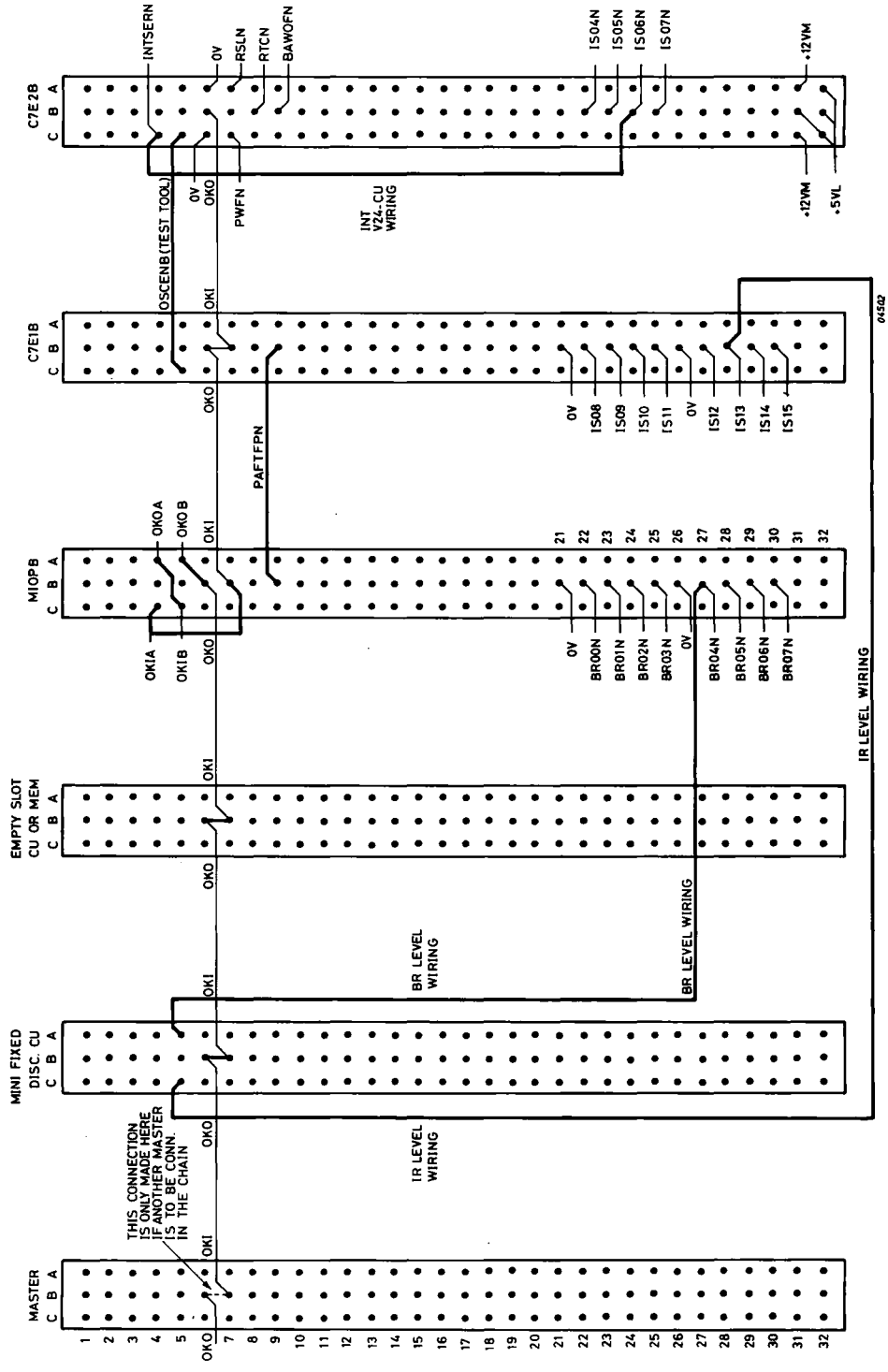


Figure 1.11 EXAMPLE OF INTERCONNECTIONS

2 FUNCTIONAL DESCRIPTION

LIST OF ILLUSTRATIONS

LIST OF TABLES

2.1 SWITCH-ON

At switch-on a sequence of events takes place before the system is ready to go, see Figure 2.1. This sequence of events may be considered as three separate phases.

. Phase 1 Automatic Test
. Phase 2 Microdiagnostic Test
. Phase 3 Load IPL (Initial Program Loader)

The hexadecimal codes of the HHCP and FRCP that are displayed after an event are indicated in the following Flow Charts.

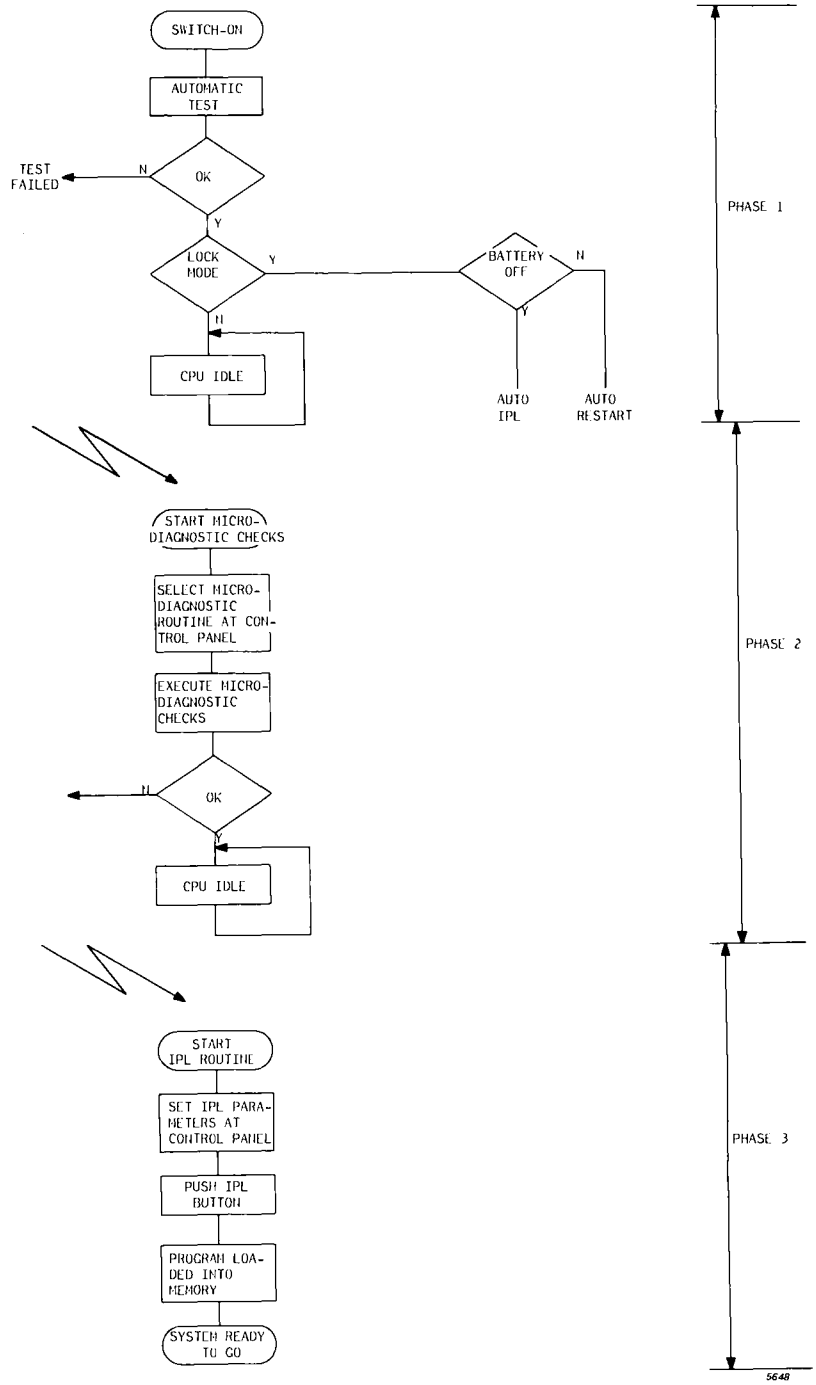


Figure 2.1 START PROCEDURE

2.1.1 AUTOMATIC TEST (Figure 2.2)

The Automatic Test is always carried out after switch-on or Master Clear. During the test the major part of the CPU, the Control Panel and the Control Panel cables are tested.

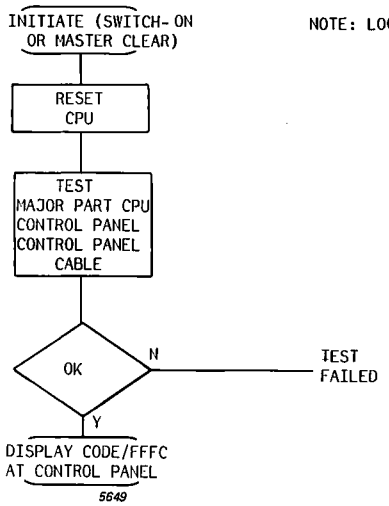


Figure 2.2 AUTOMATIC TEST

At the end of this test there are 2 possibilities:

- Test failed- code FFFC is not displayed so the diagnostic tests may not be carried out and other fault finding methods must be used to locate the fault which is either CPU, control panel, or control panel cable, or UPL BUS, or Memory.
- Test passed- code FFFC is displayed so the diagnostic tests may now be initiated.

2.1.2 MICRODIAGNOSTIC TEST (FIGURE 2.3)

The Microdiagnostic Test should be executed immediately after the Automatic Test in order to ensure the correct functioning of the system. If a fault occurs during these tests then a code is displayed at the control panel.

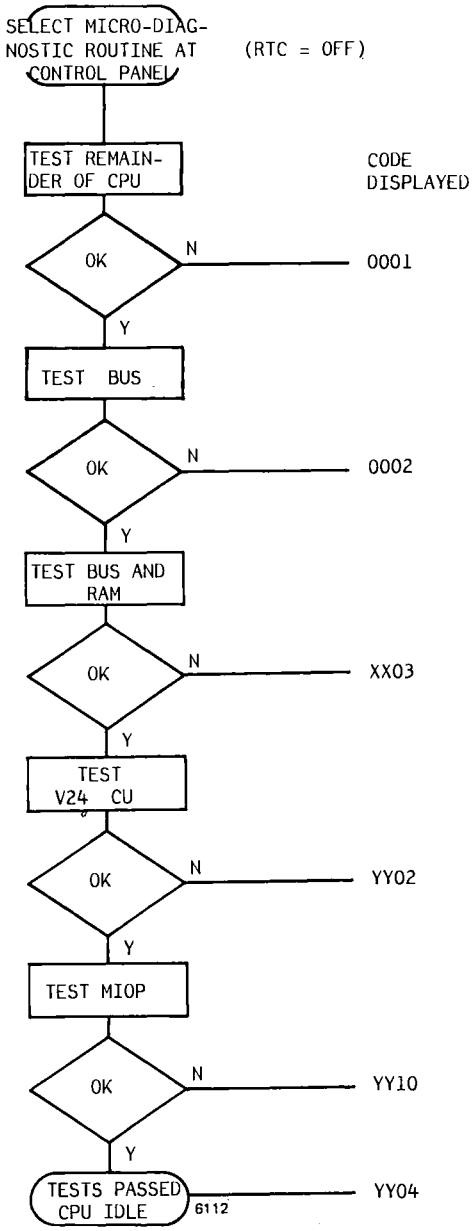


Figure 2.3 MICRODIAGNOSTIC TEST

All codes displayed are error codes except after the Bus and RAM Test is passed (YY04) where YY indicates the 8 most significant bits of the last address tested (32k max.). For the Bus and RAM Test failed (XX03) XX indicates the 8 most significant bits of the address causing the error.
The error address can also be read from register A1 and the content of this address from register A2.

2.1.3 INITIAL PROGRAM LOADER (FIGURE 2.4)

The Initial Program Loader (IPL) is responsible for system initiation by enabling the eventual loading of an Object Program. For purposes of this description the IPL Sequence to load from a Sequential Device is described in 3 parts:

. Bootstrap
. Low Core IPL
. High Core IPL

BOOTSTRAP

The Bootstrap is contained in the Bootstrap ROM in the CPU in a format 1k x 4bits. The CPU assembles this format into 256 x 16-bit words which are loaded into Memory starting from address 000. The Bootstrap enables the loading of the Low Core IPL.

LOW CORE IPL

The Low Core IPL has 3 principal functions:

. Calculates the size of Memory and subtracts 400 characters to find the High Core start address.
. Loads High Core IPL.
. Starts High Core IPL.

HIGH CORE IPL

The High Core IPL has 3 principal functions:

. Gives the peripheral address (Reg. A15) from which the Object Program is to be loaded.
. The IDENT name of the program to be printed out on the ASR.
. Loads the Object Program

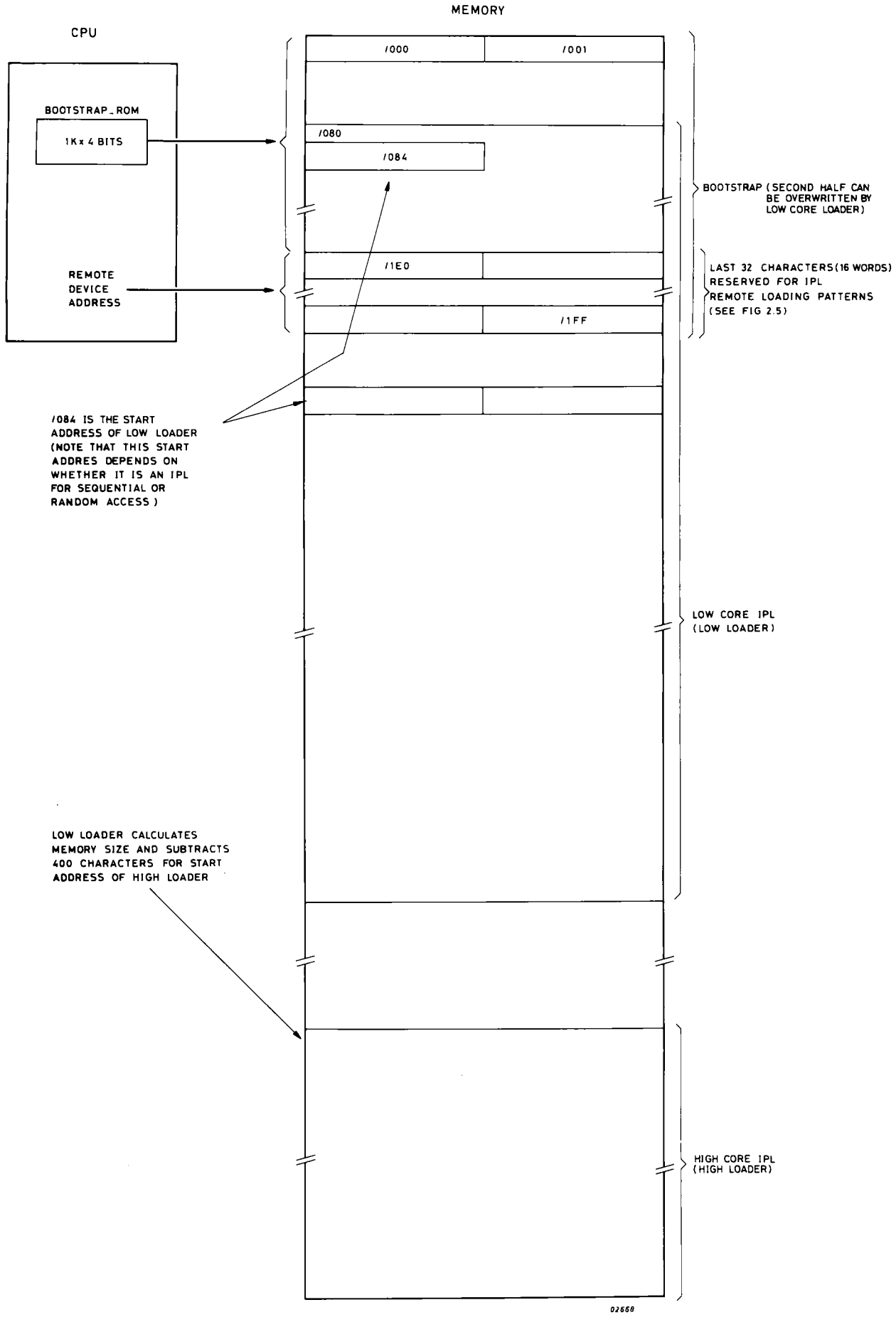


Figure 2.4 INITIAL PROGRAM LOADER - PRINCIPLE

2.1.4 LOAD REMOTE IPL (FIGURE 2.5)

The last 16 words of the Bootstrap (addresses 240-255(/1E0 to /1FF) inclusive) contain parameters for up to 16 remote devices. The system enables operation in one of two modes:

. Address is selected by card links OPSON-3N.
. Remote Device sends its own address, no links selected.

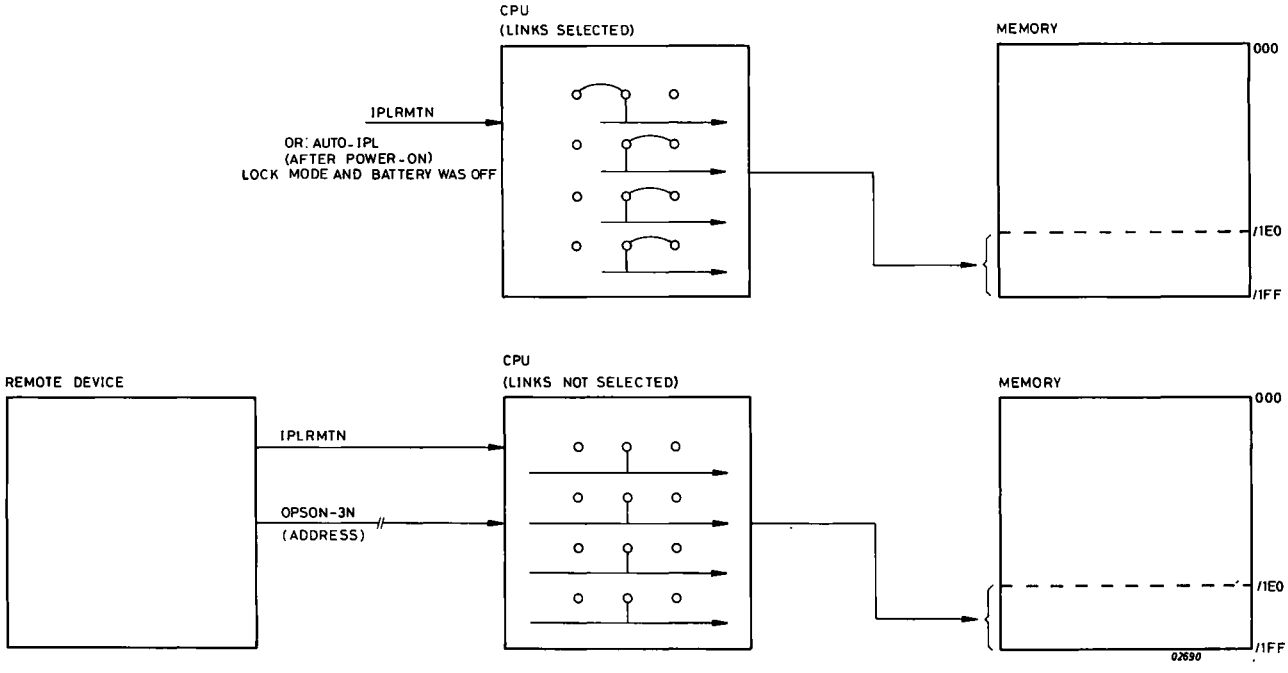


Figure 2.5 REMOTE IPL

2.2 SERIAL INTERFACES

There are two serial interfaces employed on the P857E; Control Panel and V24 Peripheral Interfaces both of which use a device type 8251A and share common functions.

2.2.1 SERIAL INTERFACES - COMMON FUNCTION

The 8251A is responsible for the conversion of data from serial to parallel and parallel to serial. Before data transfers may be carried out the interface must be programmed: this is the responsibility of the CPU Microprogram. For purposes of this explanation the sequence of events at the interface are as follows:

. Switch-On
. Program Mode Instruction
. Program Command Instruction
. Change of Command
. Reset and Reprogram

SWITCH-ON

At Switch-on the serial interfaces are both reset and so must be programmed with the Mode of Operation. This is the responsibility of the CPU Microprogram.

PROGRAM MODE INSTRUCTION

In the reset state a Mode Instruction must be executed to program the mode of operation for the interface; character length etc. see Figure 2.7.

PROGRAM COMMAND INSTRUCTION

A command instruction must follow the Mode Instruction and is used to command a particular type of operation; input or output etc. see Figure 2.7.

CHANGE COMMAND INSTRUCTION

Once the Mode Instruction is executed any number of Command Instructions may be programmed to change the type of operation. In the example of Figure 2.6 the Interface is already programmed for Output Mode but now data has to be input so another Command Instruction is programmed to specify an input operation. The Interface stays in Input until either another Command Instruction is executed or a Reset occurs.

CHANGE MODE OF OPERATION

A Mode Instruction is only executed after a Reset occurs. For the Control Panel the Modes of operation are invariable and so after a Reset (RSLN from the Power Supply or MCL from the Control Panel) the CPU Microprogram is responsible for the reprogramming of the FRCP with code /CE. The content of the V24 Mode Instruction is read from the CIO V24 Command (Figure 2.9).
The serial interface must have been reset during the CIO start command V24, before reprogramming is possible. (CPU Microprogram responsible).

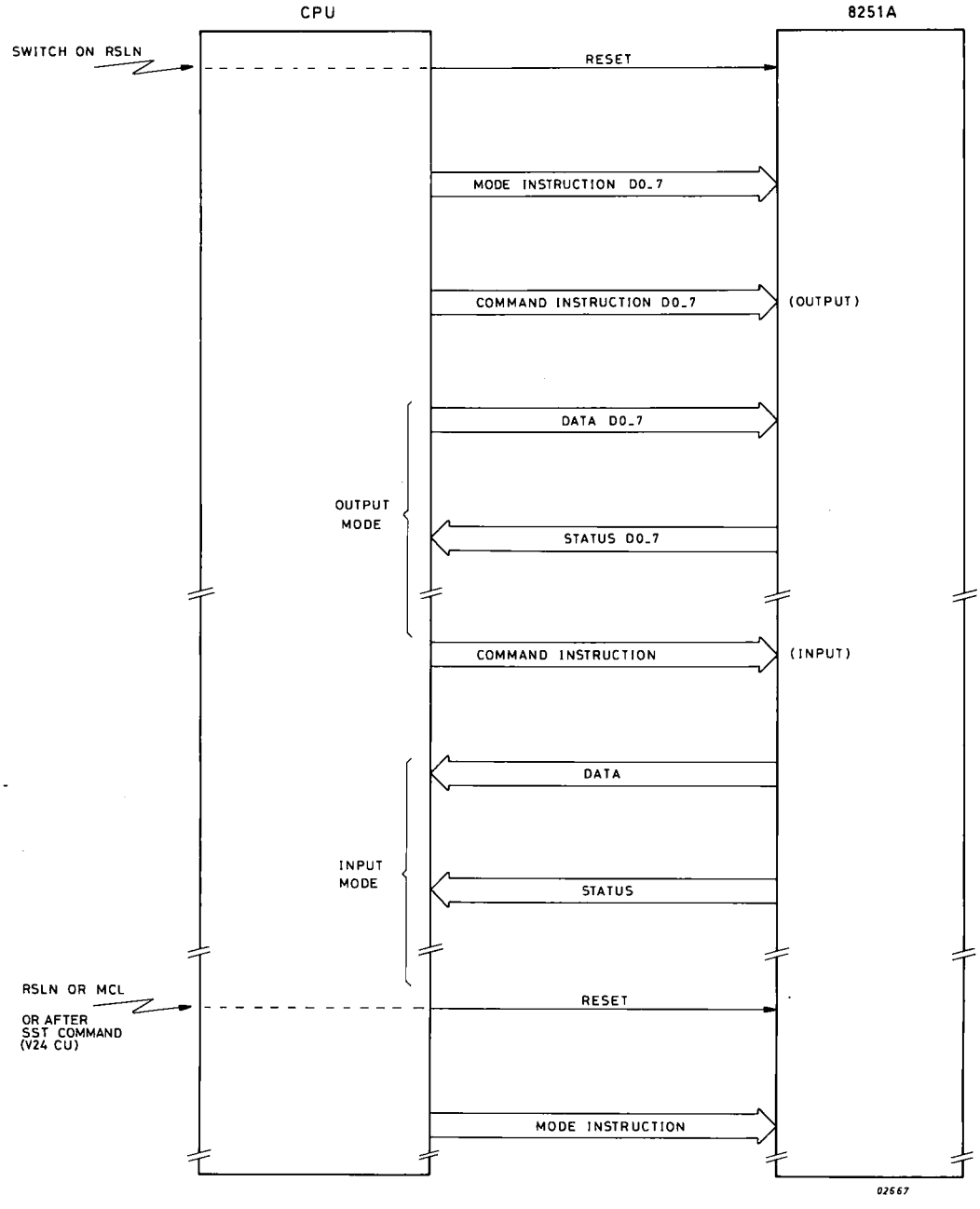


Figure 2.6 EXAMPLE OF SERIAL INTERFACE DIALOGUE

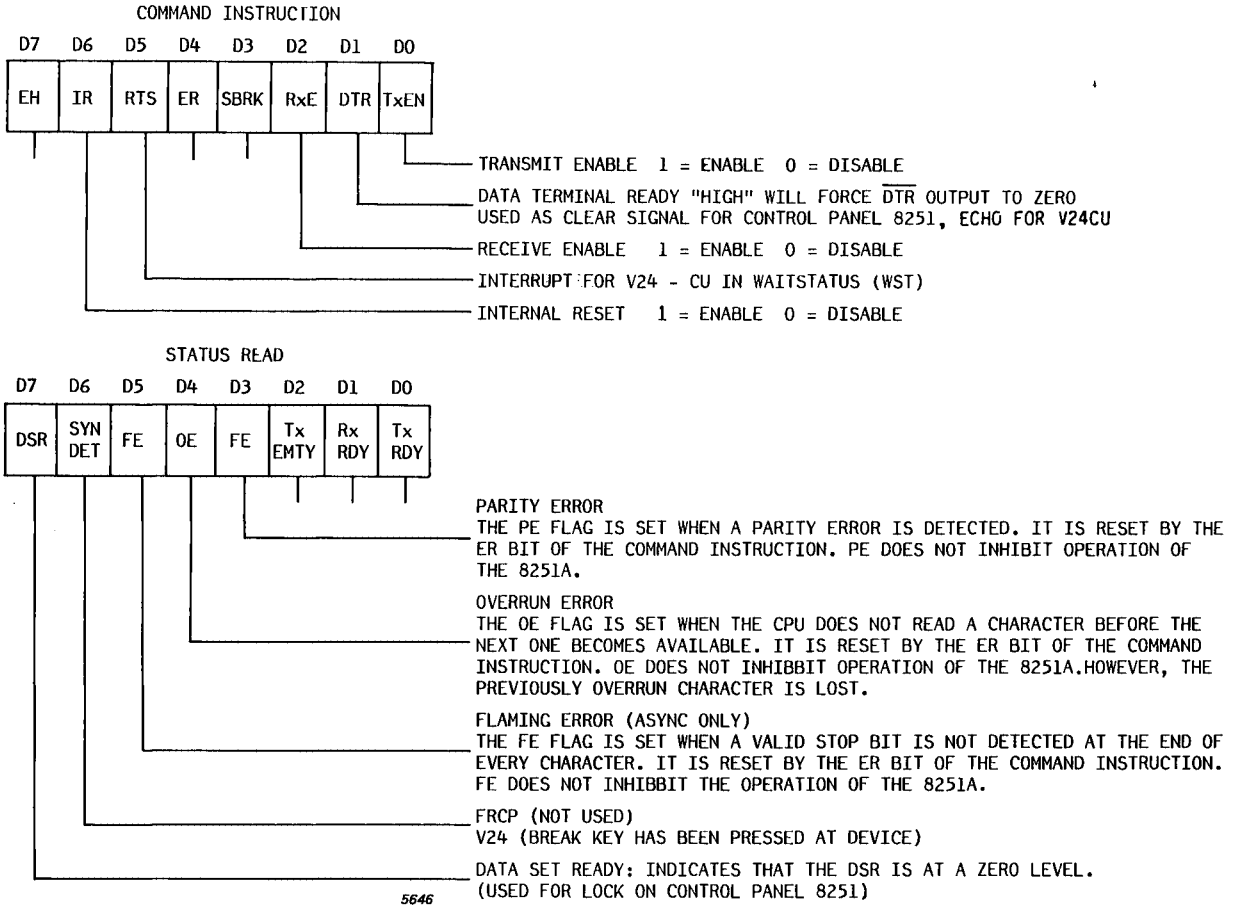


Figure 2.7 8251 CONTROL FORMATS

2.2.2 V24 PERIPHERAL INTERFACE

The V24 Interface is connected on Programmed Channel and recognises the commands shown in Figure 2.9. The V24 Interface does not use a State Sequensor but CPU tests the state of the interface during exchanges. The CPU Microprogram is responsible for synchronising the V24 Interface states (INAC, INPUT, OUTPUT, ECHO) with the overall CPU operation. The dialogue between the Serial Interface and the P857E system is shown in Figure 2.8.

2.2.3 CONTROL PANELS

One of 2 Control Panel may be connected to the P857E (Figure 2.11):

. Hand Held Control Panel (HHCP) displays hexadecimal addresses or data.
. Full Refreshed Control Panel (FRCP) displays data and address simultaneously in a hexadecimal format.

The 2 Control Panels are Micro-Processor controlled and receive data or an address in serial data format and transmit either address, data or function to the CPU. At the interface the operation and the codes transmitted to CPU are the same but the way that they are generated may differ (see Table 2.2 and figure 2.10). For purposes of this description only the FRCP is described here.

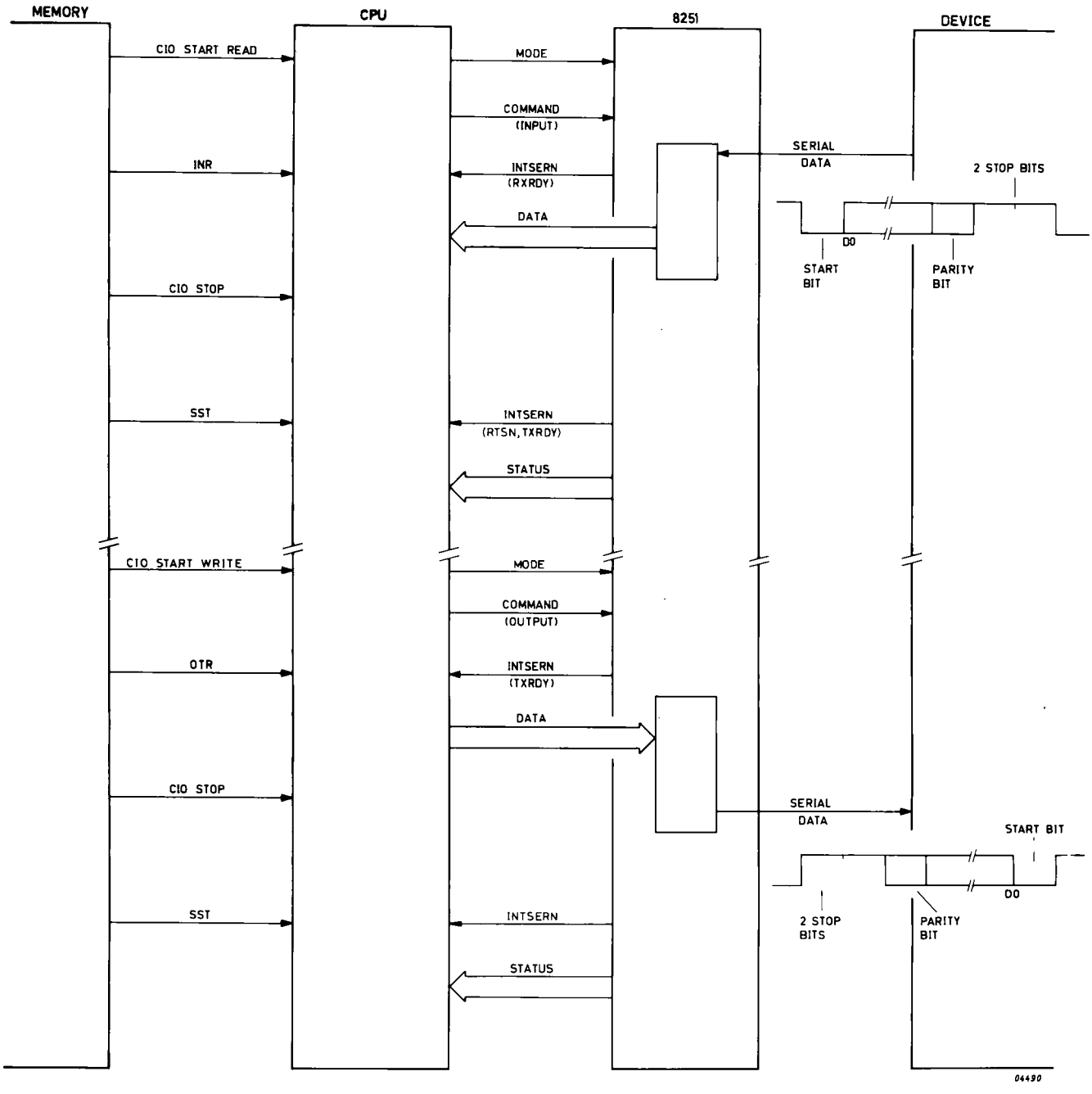


Figure 2.8 V24 PERIPHERAL INTERFACE DIALOGUES

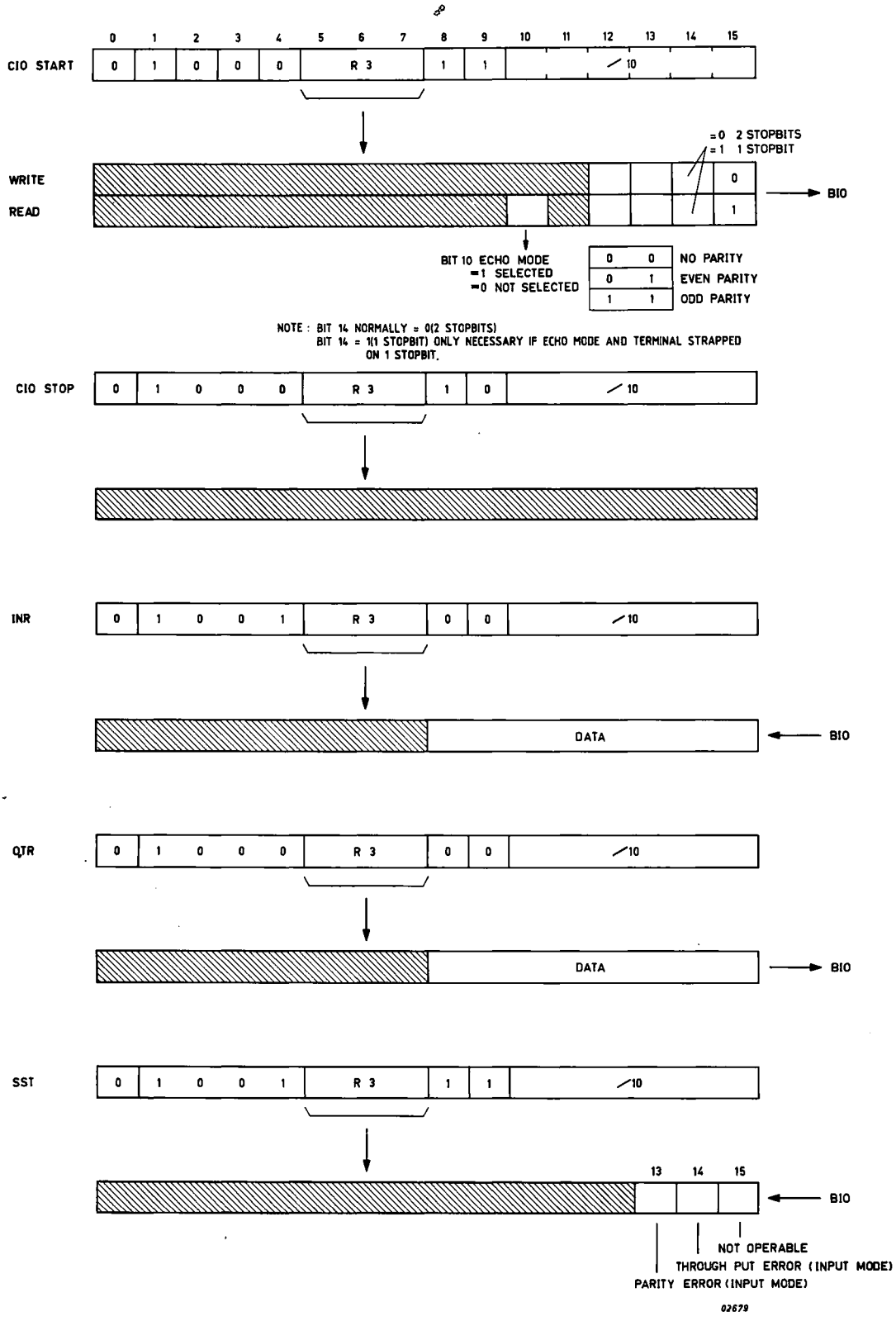


Figure 2.9 V24 PERIPHERAL COMMANDS

2.2.3.1 FULL REFRESHED CONTROL PANEL (FRCP)

The FRCP replaces the bit oriented control panels to enable the user to write and read directly in hexadecimal format.

DISPLAYS

Two set of displays one for a 6 digit address an the other for 6 digit data enables the user to read data and address simultaneously.

KEYS

There are 16 data keys and 16 function keys all of which only send the key-code to the CPU when a function key is pressed. Depending on the function the data will be coded and sent to the CPU first, followed by the function code.

EXTENDED FUNCTION MODE

The functions of the FRCP may be extended by using the "0" key in conjunction with a Function Key. The principle is shown below, and the extended functions that are available are shown in Table 2.2.

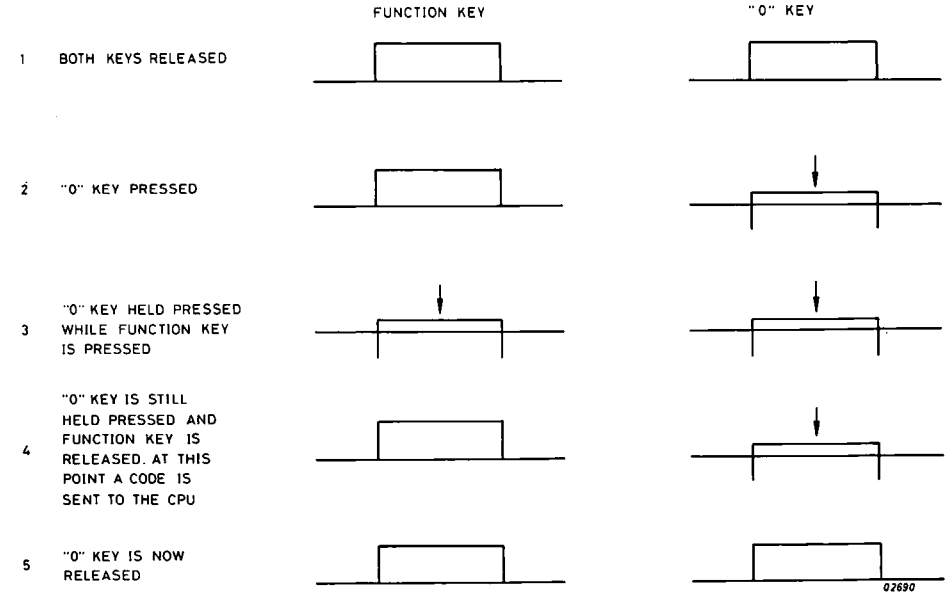
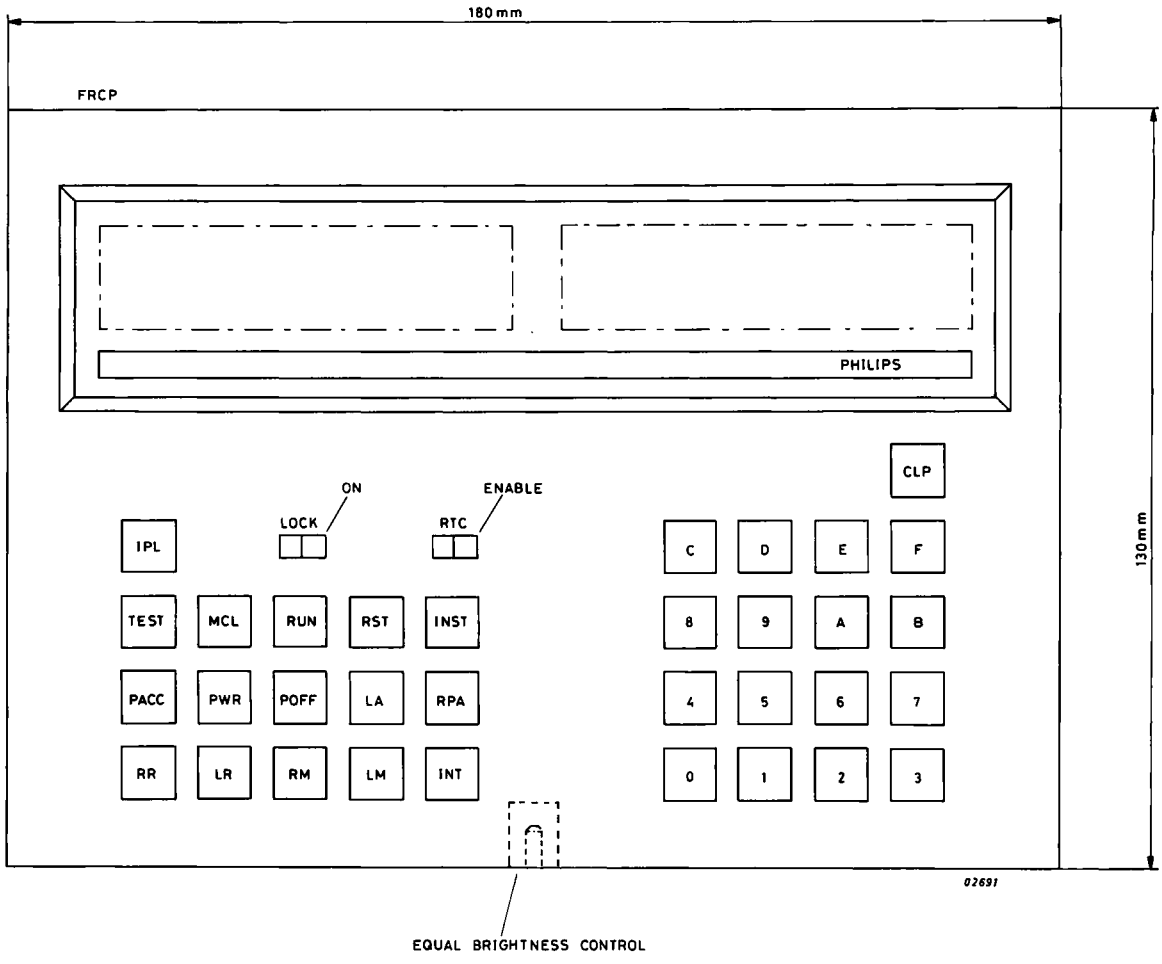


Figure 2.10 EXTENDED FUNCTION MODE

FRCP CODES

Data and functions exchanged between the FRCP and P857E are in the form of a serial 8-bits code. These codes contain the prefix 3 for data and either 4 or 5 for functions and /B for addresses. See Table 2.1.



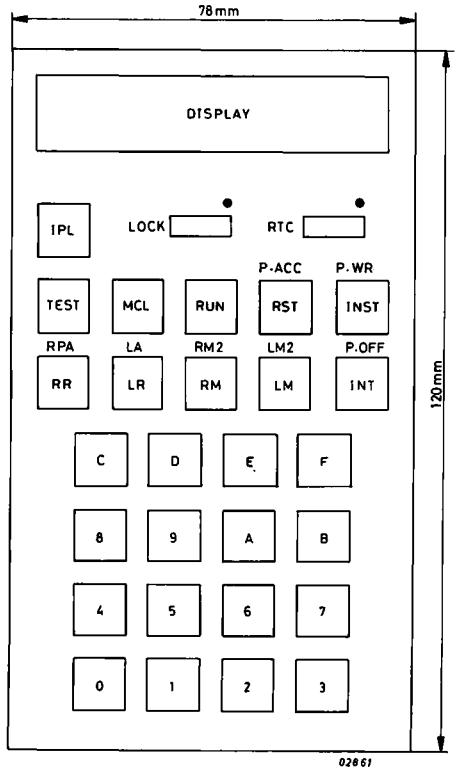


Figure 2.11 FRONT VIEW OF HHP/FRCP AND HHP AND FRCP CONTROL PANELS

The basic dialogue between FRCP and P857E is the switching between Idle and Run Modes in conjunction with the FRCP function keys. This dialogue is shown in Figure 2.12. Other dialogues exist such as the generation of signal CLEARN but this is described later in the operation of the Microprogram.

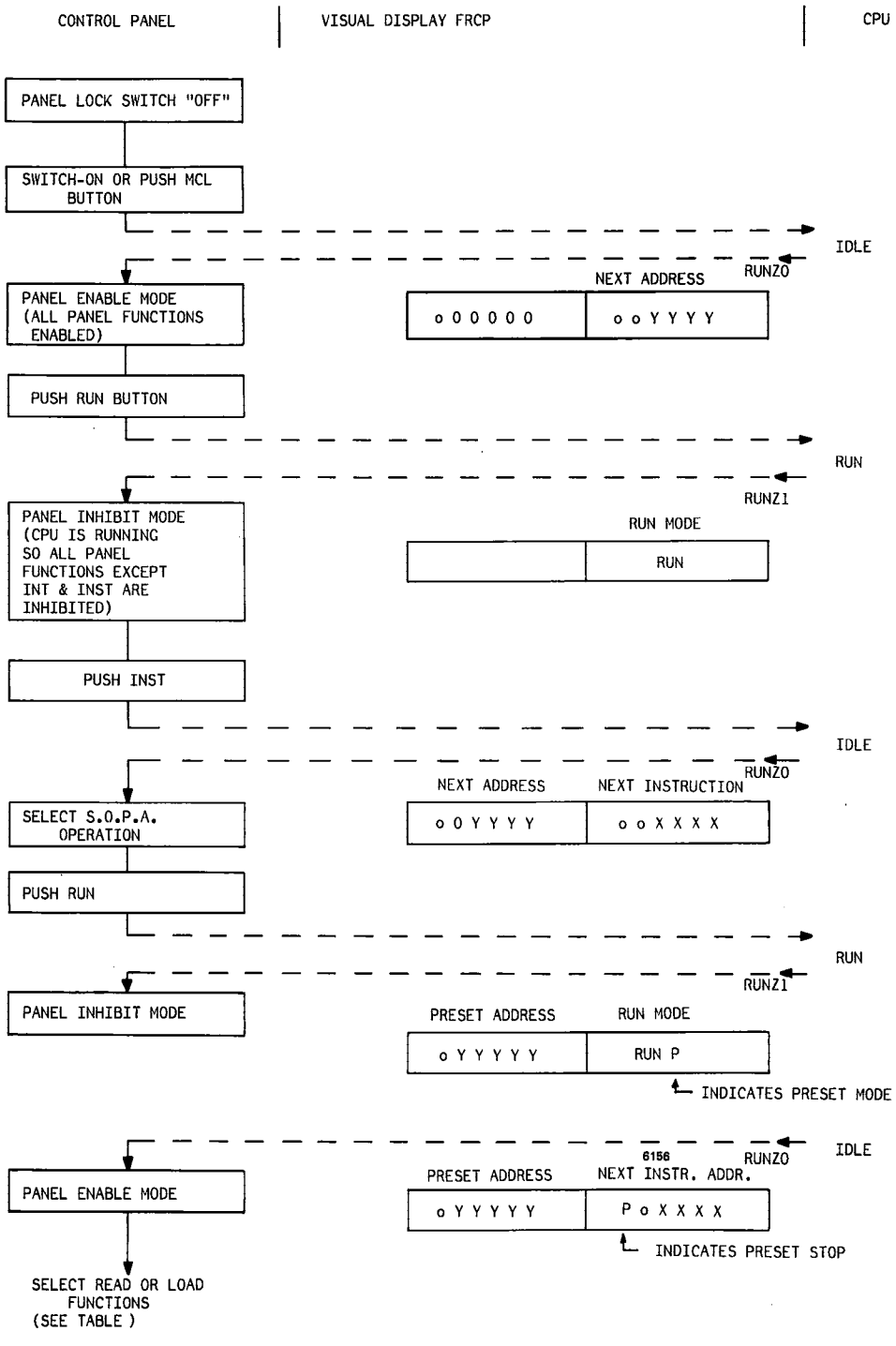
Data Value	Hex Code	Function	Hex Code
0	/30	MCL	/40
1	/31	LR	/41
2	/32	RR	/42
3	/33	RST	/43
4	/34	IPL	/44
5	/35	LM1	/45
6	/36	INT	/46
7	/37	RM1	/47
8	/38	LA	/48
9	/39	INST	/49
A	/3A	RPA	/4A
B	/3B	RUN	/4B
C	/3C	PACC	/4C
D	/3D	PWR	/4D
E	/3E	TEST	/4E
F	/3F	POFF	/4F
		LM	/55
		RM	/57

Note that addresses are prefixed by /B.

Table 2.1a TRANSMISSION CODES (PANEL to CPU)

Function	Hex. Code	Signals Name
switch from Idle to Run	/41	RUNZ1
switch from Run to Idle	/40	RUNZ0

Table 2.1b TRANSMISSION CODES (CPU to PANEL)



NOTE: THE DOTTED LINES REPRESENT THE SERIAL DATA PATHS BETWEEN THE CPU AND CONTROL PANEL.

Figure 2.12 FRCP/P857E DIALOGUE

Operation		KEYS	
		FRCP	HHCP
Read	Read Status	RST	RST
	Read Register	RR	RR
	Read Memory (pointed by Ao)	0 and RM	RM
	Read Memory (pointed by MAR*)	RM	0 and RM
Load	Initial Program Load	IPL	IPL
	Load Register	LR	LR
	Load Memory (pointed by Ao)	0 and LM	LM
	Load Memory (pointed by MAR*)	LM	0 and LM
	Load Memory Address Register	LA	0 and LR
Stop On Preset Address	Read Back Preset Address	RPA	0 and RR
	Disables SOPA Function	POFF	0 and INT
	Enable SOPA for any mem. access	PACC	0 and RST
	Enable SOPA for mem. write access	WR	0 and INST
Others	CPU Run	RUN	RUN
	System Master Clear	MCL	MCL
	Step CPU to next instruction	INST	INST
	Control Panel Interrupt	INT	INT
	Test Control Panel Data Displays	TEST	TEST
	Execute Microdiagnostic Routine	0 and TEST	0 and TEST
	Clear Control Panel Displays	CLP	NONE
	Enable/Inhibit Real Time Clock	RTCE	RTCE
	Enable/Inhibit Panel Functions	LOCK	LOCK
	Display the most significant digit (by rotation)	NONE	0 and MCL
	Equal brightness control is a screwdriver adjustment to give the same light intensity on both displays.	YES	NONE

Table 2.2 FRCP AND HHCP FUNCTIONS

* MAR = Memory Address Register

2.3 BUS PRIORITY AND CONTROL (FIGURE 2.13)

Allocation of the UPL Bus to P857E Masters is via the Bus Priority System which forms a part of the Bus Control Logic.

2.3.1 BUS PRIORITY

Two factors decide the priority of a Master in the P857E system; the OKO/OKI Chain and the signal ERQN.

OKO/OKI CHAIN

These connections are made by the user starting from CPU Card C7E2 then C7E1 , MIOP (IOPA and IOPB) and then connected to each Master in order of priority.

ERQN

This signal is sent from the Bus Controller and operates as an inhibit/enable for the Masters to which it is connected. The decision as to whether or not the signal will be connected is made at system generation time. When the signal is not connected the BUS Controller cannot stop the Master from raising a Bus Request (BUSRN) and so that Master always take priority over the CPU. (This is the case with MIOP). When ERQN is connected, if the CPU or other Master is busy it will inhibit these Masters and when the CPU is not busy then the Masters are enabled.

2.3.2 BUS CONTROL

The control of the Bus takes into account that three different levels of priority exist. The priority (as has been described in para 2.3.1) is decided at system generation time. For purposes of explaining the function of Bus Control it is only necessary to accept that three different levels exist as follows:

. CPU
. Master - ERQN enables Master or ERQN not connected
. Master - ERQN inhibits Master

The CPU always takes the Bus when it is free and there is no Bus Controller action. When a Bus Request (BUSRN) is received, this indicates to the CPU BUS controller that one of its system Masters is requesting the Bus and so a sequence of events is initiated. For purposes of this description these events are as follows:

. No Bus Requests
. Master requests control of the Bus
. Search For Master that initiated request
. Master Selected
. Exchange in Progress
. End Exchange

NO BUS REQUESTS

When no Bus Requests are present (BUSRN = 1) the CPU automatically takes the Bus.

MASTER REQUESTS BUS

Before a Master may request the Bus (BUSRN = 0); no other Master may be selected (MSN = 1).

SEARCH FOR MASTER REQUESTNG BUS

When a Master requests the Bus, the Bus Controller immediately responds by sending OKO = 1 to search for the requesting Master. Signal OKO is passed between Masters in order of priority until it reaches a requesting Master. The Master is found so signal OKO is blocked at this Masters output so blocking the Priority Chain. This Master is now selected.

MASTER SELECTED

When the Master is selected signal MSN = 0 is sent from this Master and received by the others. In this way MSN inhibits the other Masters from raising a Bus Request.

EXCHANGE IN PROGRESS

The logic levels of the Bus Control signals during the Exchange are shown in Figure 2.14. During an exchange as soon as signal MSN goes high then another Master may request the Bus and so a second Bus allocation may be made by the Bus Controller.

END OF EXCHANGE

At the end of an exchange with no other Masters requesting the Bus, the Bus Controller automatically give the Bus to the CPU.

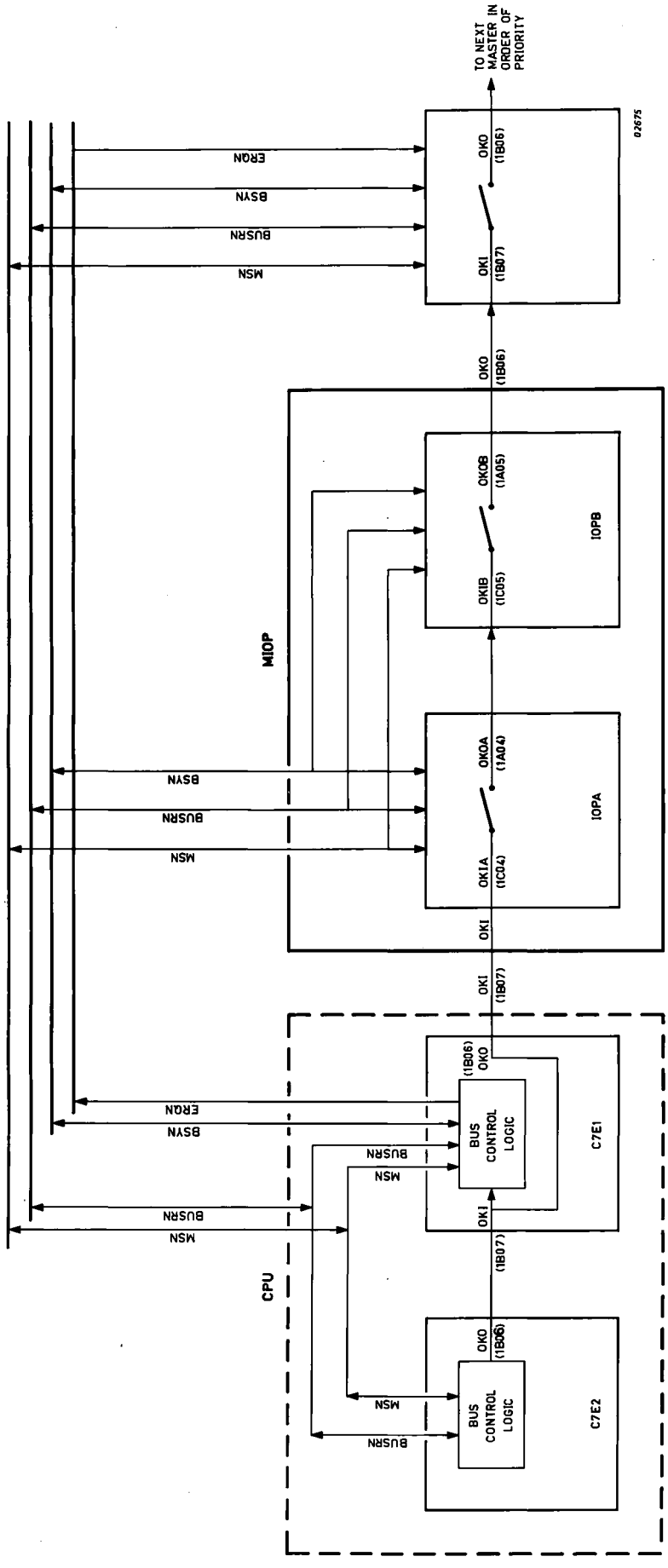


Figure 2.13 UPL-BUS PRIORITY CONTROL

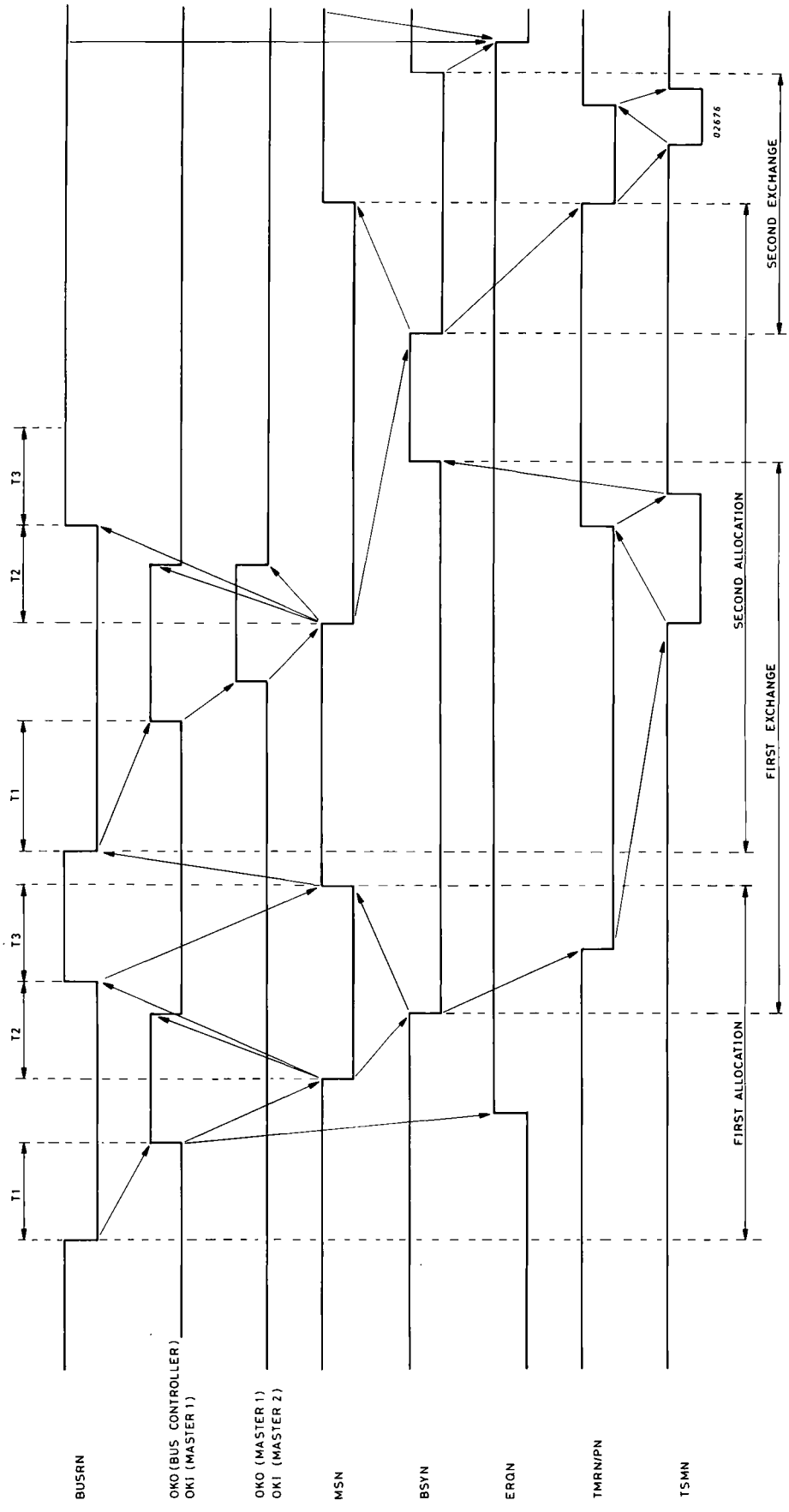


Figure 2.14 EXAMPLE OF 2 BUS ALLOCATIONS

2.4 DATA TRANSFERS

For a data transfer to take place the Bus Controller has already handed over the Bus to one of the system Masters . There are three types of Masters and so three types of data transfer possible (Input/Output):

. CPU - Programmed Channel.
. IOP - Direct Memory Access via the Input/Output Processor (Multiplex Channel).
. DMACU - Direct Memory Access via one dedicated Channel.

2.4.1 PROGRAMMED CHANNEL (FIGURE 2.15)

The programmed Channel enables data exchanges from the C.U. to CPU register (INR) or from CPU register to C.U. (OTR) under control of the CPU. Each has its own exchange request line (Interrupt) which is allocated a priority at system generation time. For purposes of this description the events at the interface are as follows:

INITIALISE C.U.

A CIO Start Instruction is executed to prepare the C.U.

START DATA TRANSFERS

When the C.U. is in EXCH an Interrupt is sent to the CPU and an OTR/INR is executed.

STOP DATA TRANSFERS

Transfers continue under control of the Interrupt and OTRs/INRs until a CIO Halt is executed. The C.U. responds with a Status Request (Interrupt) to the CPU. The C.U. status is read by executing an SST command and the C.U. switches to INACTIVE state.

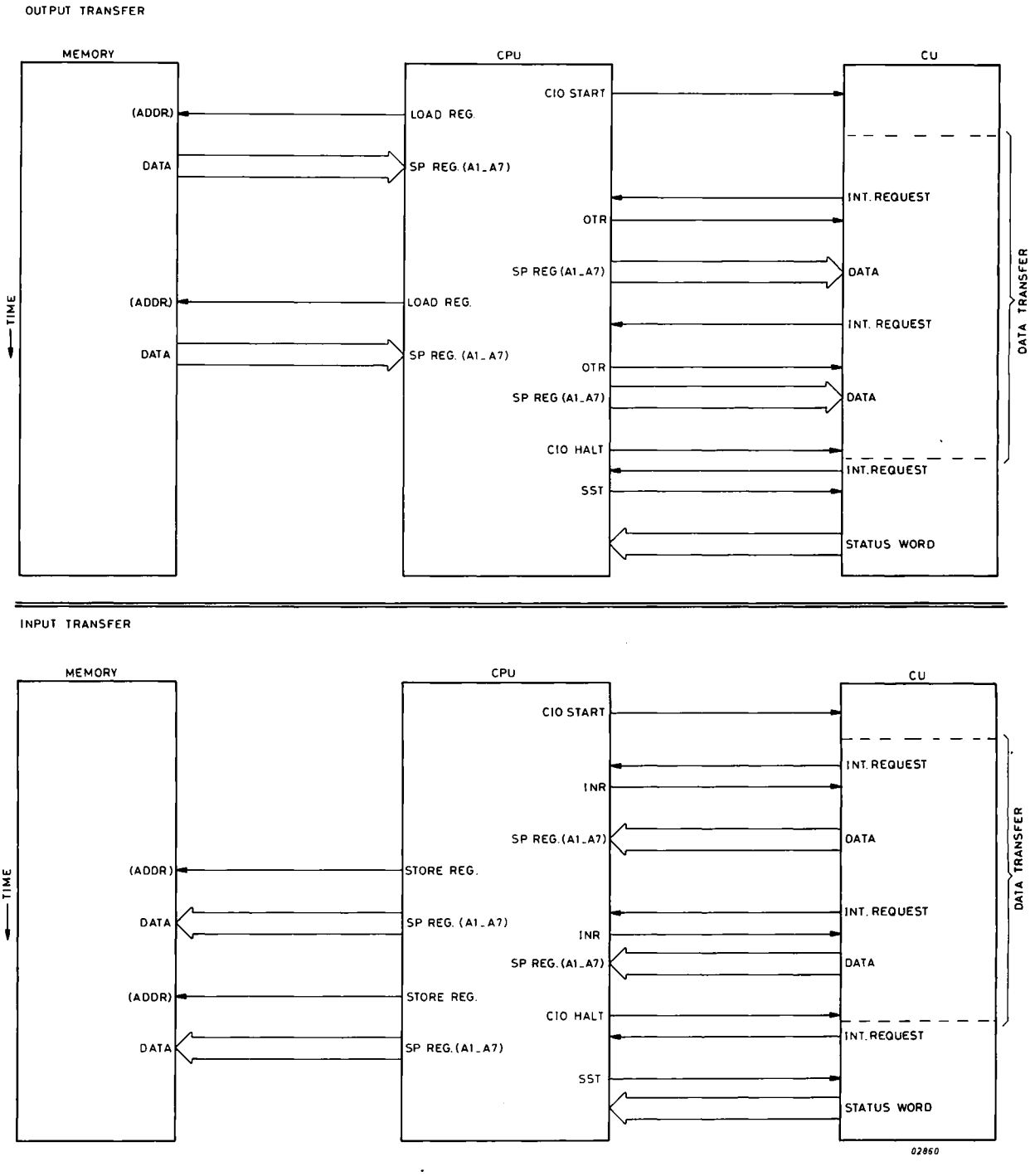
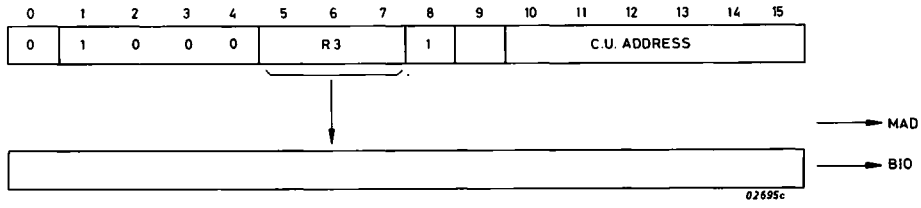


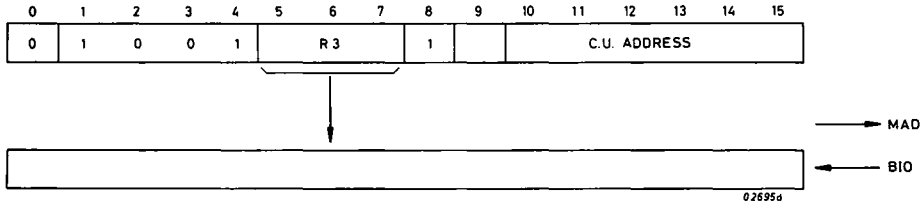
Figure 2.15 INPUT AND OUTPUT PROGRAMMED CHANNEL TRANSFERS

CIO Start and Stop Instructions



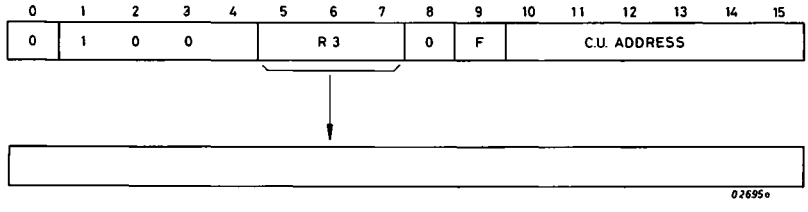
Bit 9 = 1 Start I/O operation with C.U. addressed
Bit 9 = 0 Stop I/O operation with the C.U. addressed
The content of R3 may or may not be significant depending on the C.U.

Status Instructions



Bit 9 = 1 Send status of C.U. to R3 (SST)
Bit 9 = 0 Test C.U. data sent to R3 (TST)
The content of R3 differs between C.U.s.

Data Exchange Instructions



Bit 4 = 1 Data is input to Register specified by R3 (INR)
Bit 4 = 0 Data is output from Register specified by R3 (OTR)
Bit 9 may be used to specify a particular function depending on the peripheral used.

Figure 2.16 PROGRAMMED CHANNEL COMMAND FORMATS

2.4.2 IOP CHANNEL

Input Output Processor (IOP) Exchanges (Figure 2.17). The IOP Channel enables a number of Control Units to have via IOP memory access. The MIOP houses two IOPs (IOPA and IOPB) each of which may multiplex up to 8 Control Units. Each Control Unit has its own exchange request (Break) which is allocated a priority at system generation time. For purposes of this description the sequence of events at the interface are as follows:

INITIALISE IOP

WER 1,2,3 are executed to load the exchange parameters for the C.U. into the IOP Scratch Pad: Note that WER 3 is only used when the address exceeds 18 address bits.

START DATA TRANSFERS

Once the IOP is initiated the CPU is free to carry out other operations and the IOP takes over the responsibility for the transfer. Data exchanges are now ready to take place; the C.U. activates its Break Request when it is ready for a transfer and the IOP simulates an INR or OTR to enable the exchange between C.U. and Memory.

STOP DATA TRANSFERS

Transfers continue under control of the Break and simulated INRs/OTRs until IOP recognises that the data block is transferred. The IOP indicates end of transfer (MAD03) at the same time as the last INR/OTR and the C.U. responds with a Status Request (Interrupt) to the CPU and after execution of SST the CU goes to INACTIVE state.

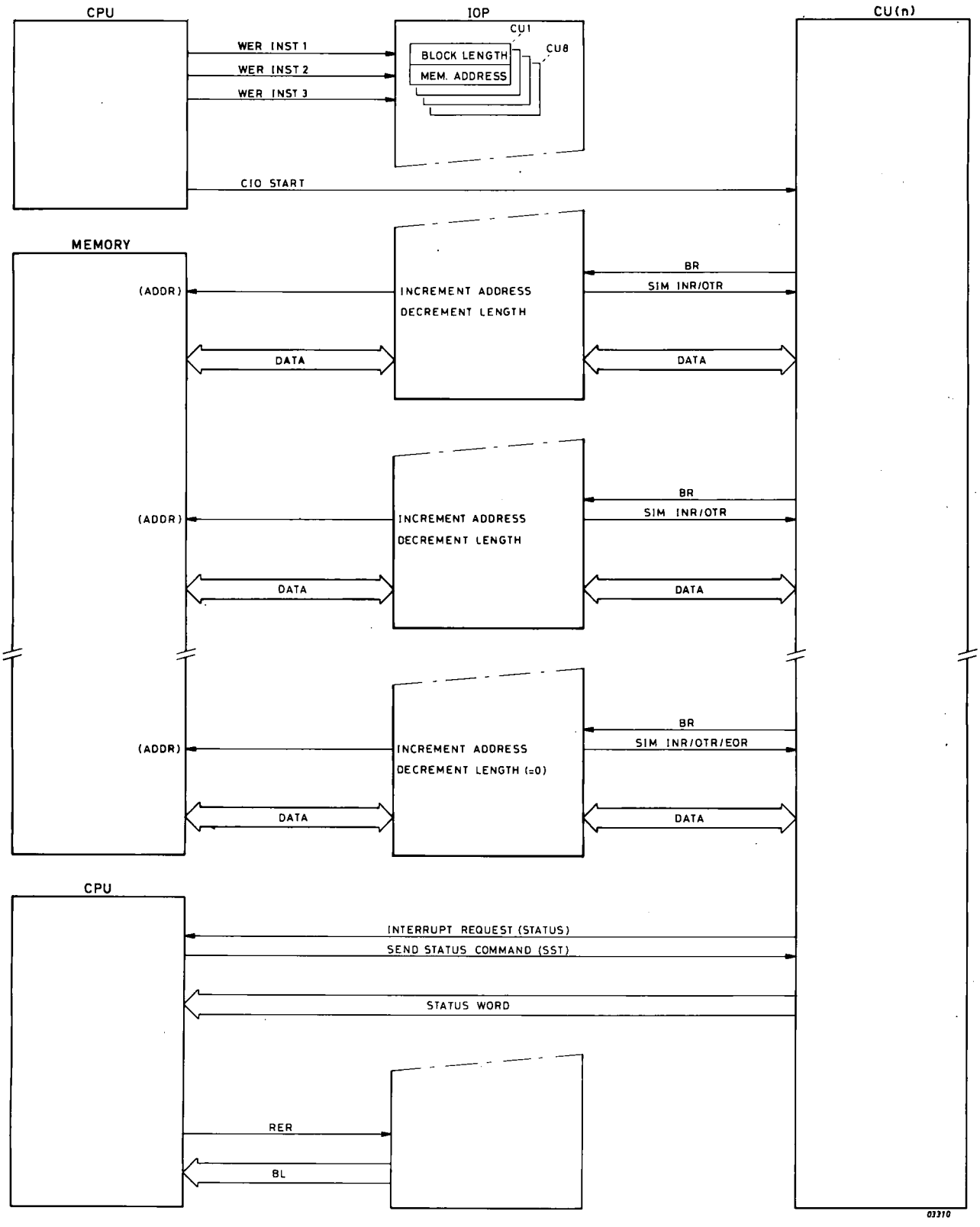
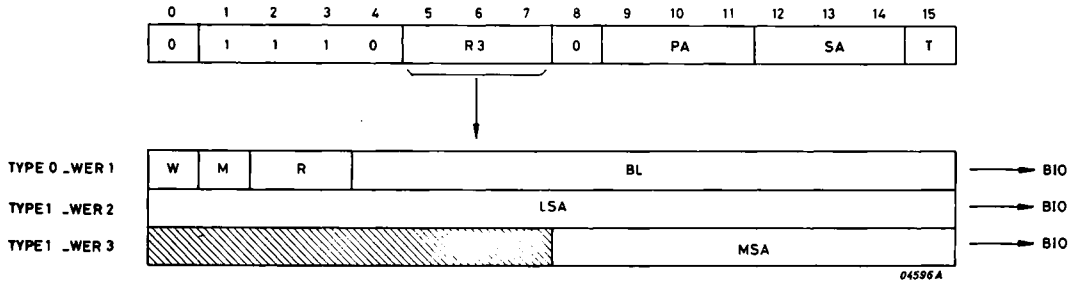


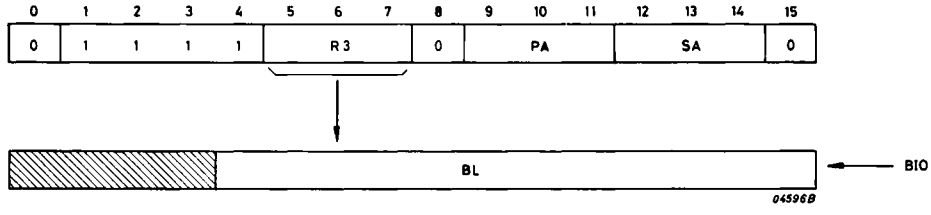
Figure 2.17 IOP CHANNEL TRANSFERS

Write External Register Instructions (WER)



PA IOP Address; for IOPA always 000, IOPB 001
SA Sub-channel address linked to PA to give the 6-bit C.U. address.
T Type of WER = 0 type 0 (WER 1), = 1 type 1 (WER 2 and 3).
W Word Transfer Indicator: = 0 transfer is an 8-bit character
M Output Mode: = 1 direction of exchange is memory to C.U.
R Address Bits and MADE6 and MADE7. If WER 3 is used these bits are overwritten by the MSA Field.
BL 12-bit block length: depending on W the block length is eiher a number of words or charcters. When BL = 0 the length is 2^{12} words or bytes.
LSA Least significant bits of the memory start address of the block to be read or written.
MSA Most significant bits of the memory start address. (MADE0-7).

Read External Register Instruction (RER)



PA IOP Address: for IOPA always 000, IOPB 001
SA Sub-channel address: linked to PA to give the C-bits C.U. address.
BL Indicates the remaining length to be transferred.

Note: CIO Start, SST and TST Commands are shown in Figure 2.16.

Figure 2.18 IOP COMMAND FORMATS

2.4.3 DIRECT MEMORY ACCESS CHANNEL (FIGURE 2.19)

The DMA Channel enables a high speed control unit to make direct exchanges with memory. The following figure 2.19 shows the sequence of events for a DMA transfer. The principle of operation is the same as for the IOP but as only one device is used the IOP/CU function is incorporated in the DMACU.

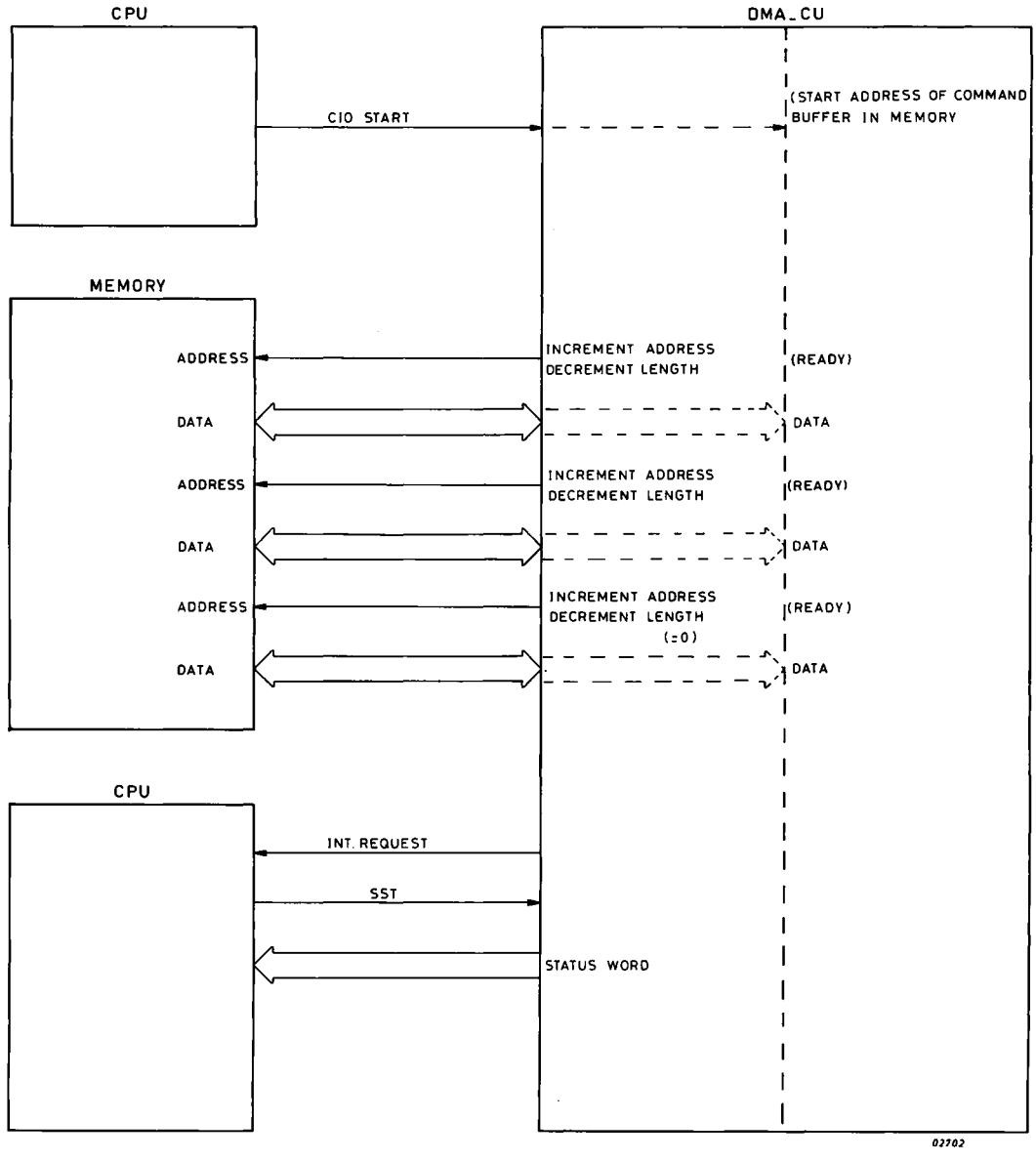


Figure 2.19 DIRECT MEMORY ACCESS CHANNEL TRANSFER (EXAMPLE CDC CONTROLLER)

2.5 UPL BUS EXCHANGES

Exchanges on the UPL Bus must respect the timing as shown in the Figures 2.20 and 2.21. When connecting a configuration the following notes must be taken into account:

. P851 Control Units - Masters connected to the UPL must take into account that signal ACN may be defined at the Master level 95nS after TSMN = 0.
. P851 Memories - Not suitable for P857E configurations except type GMB1 (with MAD extension Lines) selected in P851 mode.
. UPL Memories - Masters working on the UPL Bus may generate TMRN after T1 = 25 nS.
. MAD Lines - For the UPL Bus the MAD Lines must stay valid until TSMN = 1. The P857E employs a Double Buffer System for the MAD lines, to allow faster resynchronization of uProgram.

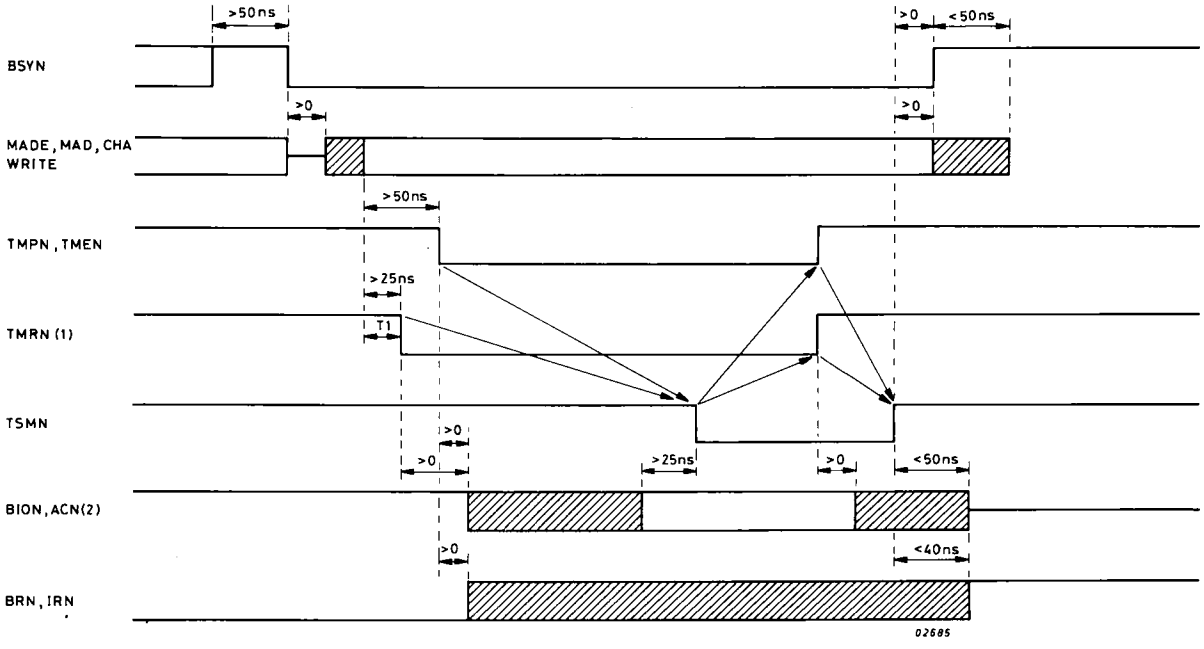


Figure 2.20 SLAVE TO MASTER EXCHANGE

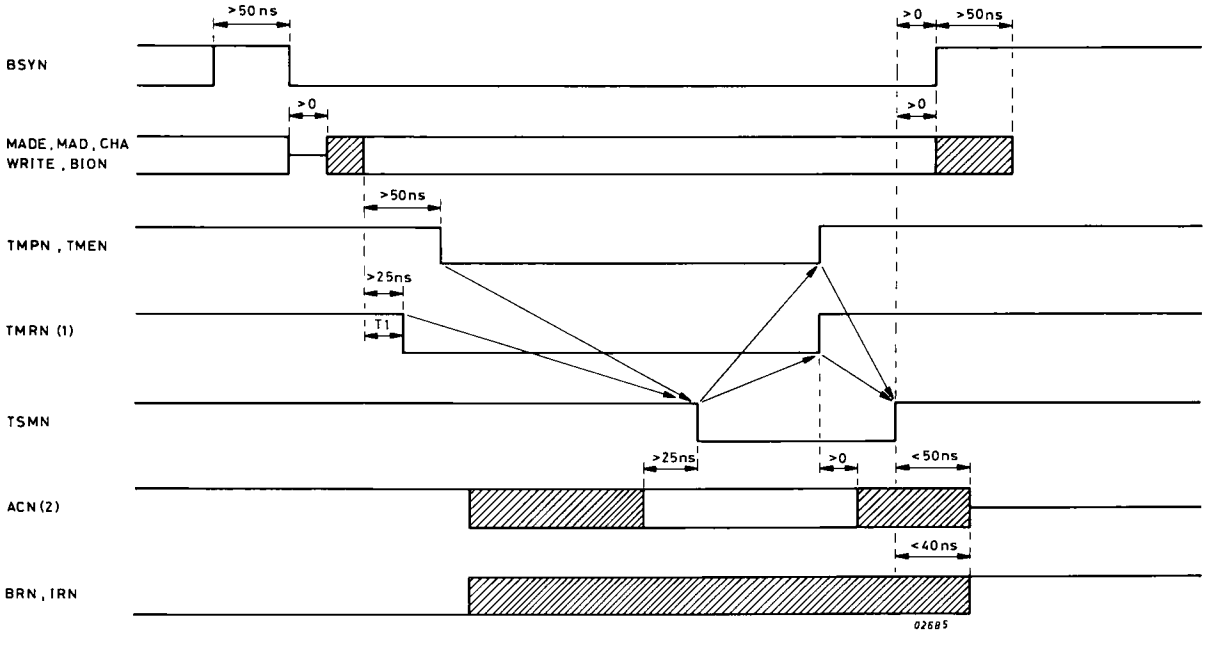


Figure 2.21 MASTER TO SLAVE EXCHANGE

2.6 INTERRUPTS

The P857E interrupt System accepts two types of interrupt from its System Control Units:

. Parallel interrupts of the GPBS (P851) Control Units
. Serial interrupts of the UPL Control Units

Although the generation and receptions of these interrupts is different at the Interface Level the CPU encoding logic processes both of them as a 6-bit code. This interrupt code indicates to the CPU that a certain action is required. The P857E accepts up to 64 interrupt levels of which 4 are internal to the CPU and 3 are Traps. The organisation of the Interrupt Control Addresses is shown in Figure 2.22.

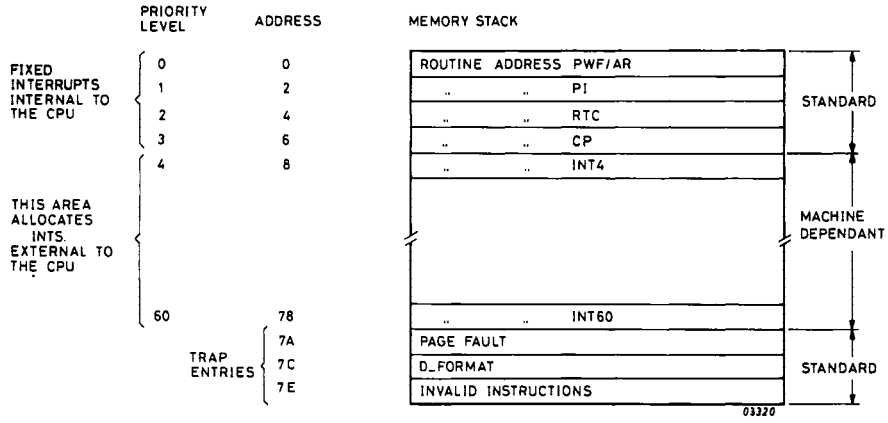


Figure 2.22 SYSTEM INTERRUPT CONTROL ADDRESSES

2.6.1 INTERNAL INTERRUPTS

The four internal interrupts (levels 0-3) are fixed. The priority levels shown in Figure 2.22. When active, a F/F internal to the CPU is latched and this F/F must be reset with an RIT instruction (Reset Internal Interrupt) during the interrupt routine.

EXTERNAL INTERRUPTS

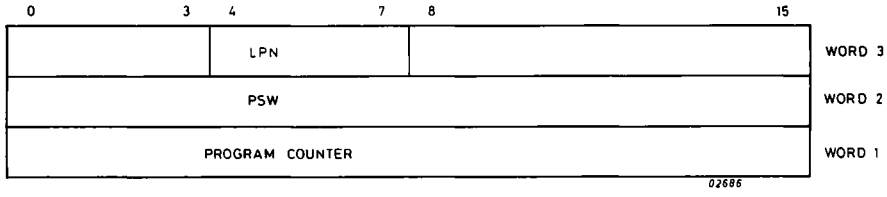
These interrupts are associated with I/O systems and may be used in general in any of the following circumstances:

. Request for data exchange (only if not connected to IOP-channel)
. Request for status exchange
. Indication ready after not ready (in fact status: Ready interrupt)

TRAPS

The Trap mechanism is similar in principle to the interrupt system except that when it is activated it does not take account of the PLR content or whether the CPU is in Enable/Inhibit interrupt mode. The CPU activates the Trap mechanism when the following conditions occur:

. Page Fault (Memory access fault) - generated by th CPU when in User Mode because the NMU has indicated to the CPU that a Page Fault has occurred. The CPU initiates a Page Fault Micro-Routine and during this routine 3 words are saved in the System Stack in the following format. See also Figure 2.26.



LPN = LOGICAL PAGE NUMBER

. Format D - This Trap may be used so that software can simulate Format D instructions. During this routine only words 1 and 2 are saved.
. Invalid Instruction - This Trap is executed for any type of abnormal of an instruction which include:
. non-recognised instructions
. priveledged instructions executed in User Mode.
. system stack access in user mode

During this routine only words 1 and 2 are saved.

2.6.2 INTERRUPT ACTION (FIGURE 2.23)

At power-on time or Master Clear all interrupts are reset and the CPU is in Enable Interrupt Mode. In this mode the CPU continually scans the interrupt lines for an interrupt request. When the interrupt is received a sequence of events is initiated to service the interrupt, these events are shown in Figure 2.23.

2.6.3 BINARY CODED INTERRUPTS

The P857E has the facility to receive binary coded interrupts in the format shown in Figure 2.24. The P857E uses only the Source code, the values of the Destination and Function are ignored and are fixed at binary 1. The Source Code gives the Interrupt Level of the Control Unit requesting the transfer. When the serial interrupt line or BCI (Binary Coded Interrupts) is not active (level 0) any Control Unit may send a serial interrupt and it is possible for a number of Control Units to start to send their interrupt at the same time. As shown in Figure 2.24, when 3 Control Units start to transmit by only Control Unit B completes because it has the highest priority. If a Control Unit tries to send a "1" but detects that a "0" is already on the Line its output circuit is reset but remains ready to try again after 16 INCL pulses are received. The 16 INCL pulses represent the count for one Binary Coded Interrupt.

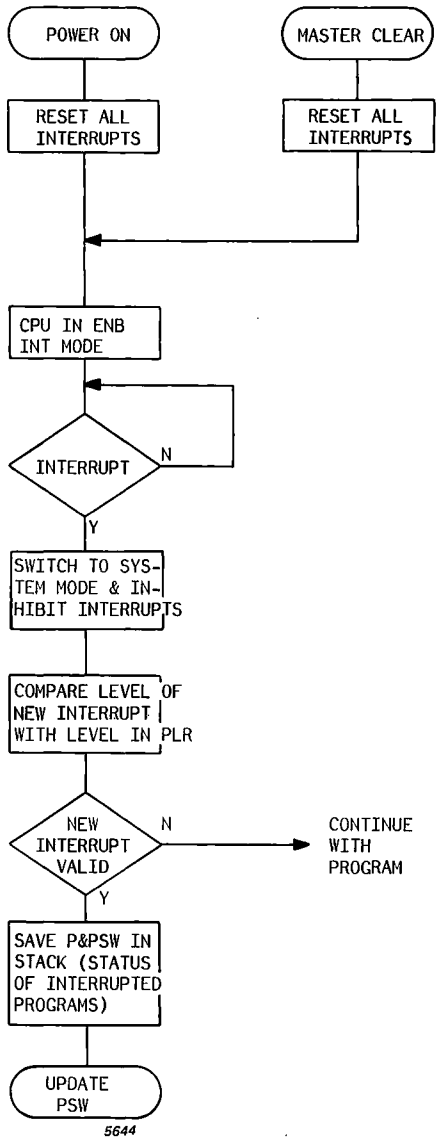


Figure 2.23 INTERRUPT ACTION - PRINCIPLE

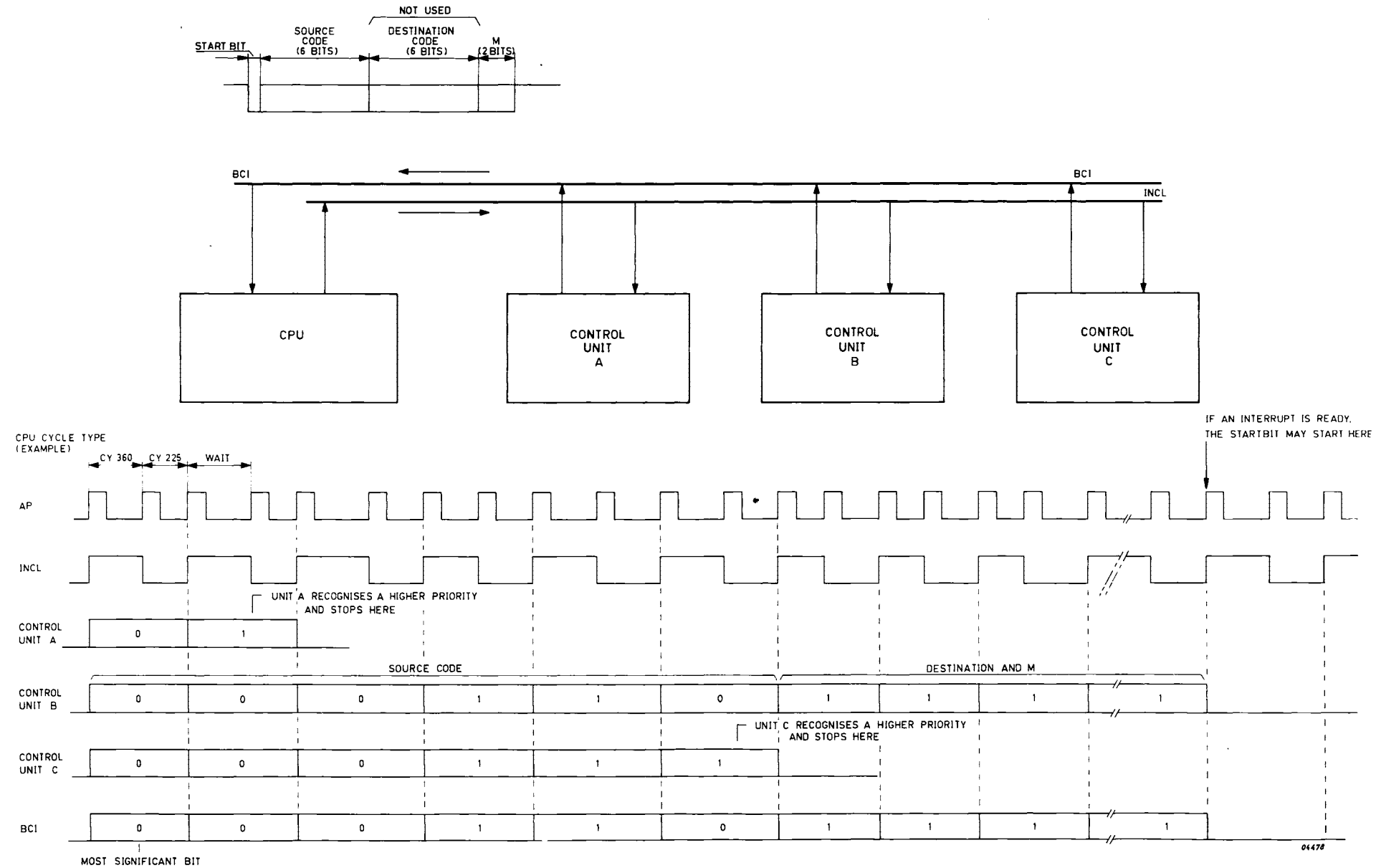


Figure 2.24 SERIAL INTERRUPTS - PRINCIPLE OF OPERATION

2.7 MEMORY MANAGEMENT UNIT

The Memory Management Unit (MMU) is a hardware facility which provides extended memory addressing and memory protection facilities for the P857E system.

2.7.1 EXTENDED MEMORY ADDRESSING (TRANSLATION)

The principal function of the MMU is to extend the memory addressing up to 8M physical words (24 address bits).
The basic rules for the operation of this facility are as follows:

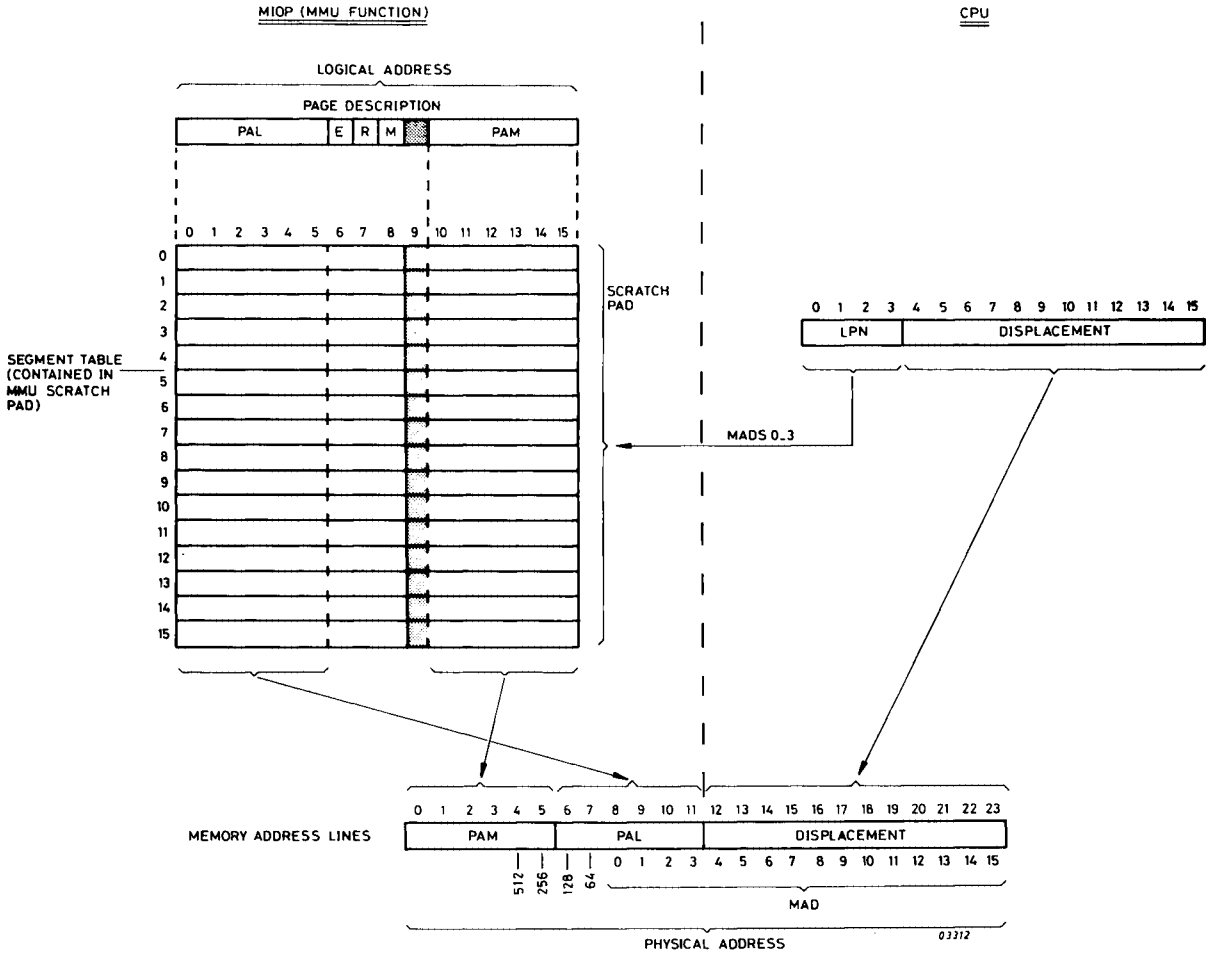
- A sixteen table segment is pre-loaded with page addresses by one Table Load instruction.
- All CPU/Memory transfers via the MMU use the four most significant address lines (MADS0-3) to select the table segment (page 0-15). The content of each page gives the 12 most significant MAD address bits plus 3 control bits.
- The Table Store instruction is used by software to read the 16 word segment table for test purposes or for dynamic relocation.

2.7.2 MEMORY PROTECTION

For memory protection purposes 2 information bits are loaded into the segment table at the same time that the TL instruction loads the page addresses; these information bits are:

- Bit 6 (E) Page Error, if 1, page restricted to system mode only.
- Bit 7 (R) Read Only Indicator = 1 to protect the page against Write operations. If an address translation in User Mode attempts to Write on this page then the translation is blocked.

In both of these cases the MMU indicates to the CPU that a Page Fault (PAF) has occured.



ABBREVIATIONS

PAL	—	PAGE ADDRESS LEAST SIGNIFICANT
PAM	—	PAGE ADDRESS MOST SIGNIFICANT
E	—	PAGE ERROR. = 1 EXCEPT FOR MEMORY RESIDENT PAGES OF USER PROGRAM
R	—	READ ONLY INDICATOR; = 1 TO PROTECT THE PAGE AGAINST WRITE OPERATIONS
M	—	MODIFIED INDICATOR. = 1 WHEN A WRITE OPERATION IS PERFORMED FOR THAT PAGE
LPN	—	LOGICAL PAGE NUMBER
DISPLACEMENT	—	GIVES THE ADDRESS RELATIVE TO THE BEGINNING OF THE LOGICAL PAGE NUMBER
MAD	—	MEMORY ADDRESS LINES

Figure 2.25 MEMORY MANAGEMENT

2.7.3 MODIFIED PAGE

This feature indicates to the operating system if a page needs to be "swapped out" or not. If it does not need to be "swapped out" then the new page can be overwritten so saving time. This possibility is indicated by bit 8 (M) which is set to "1" by the MMU whenever a Write operation (Store Instruction) is performed on a specific page.

2.7.4 PAGE FAULT

When an attempt is made to write into a protected page or access is made in user mode to a page that is restricted to system mode only, the MMU signal "Page Fault" initiates an interrupt TRAP Routine at the CPU. The sequence of events is indicated in the following Flow Chart:

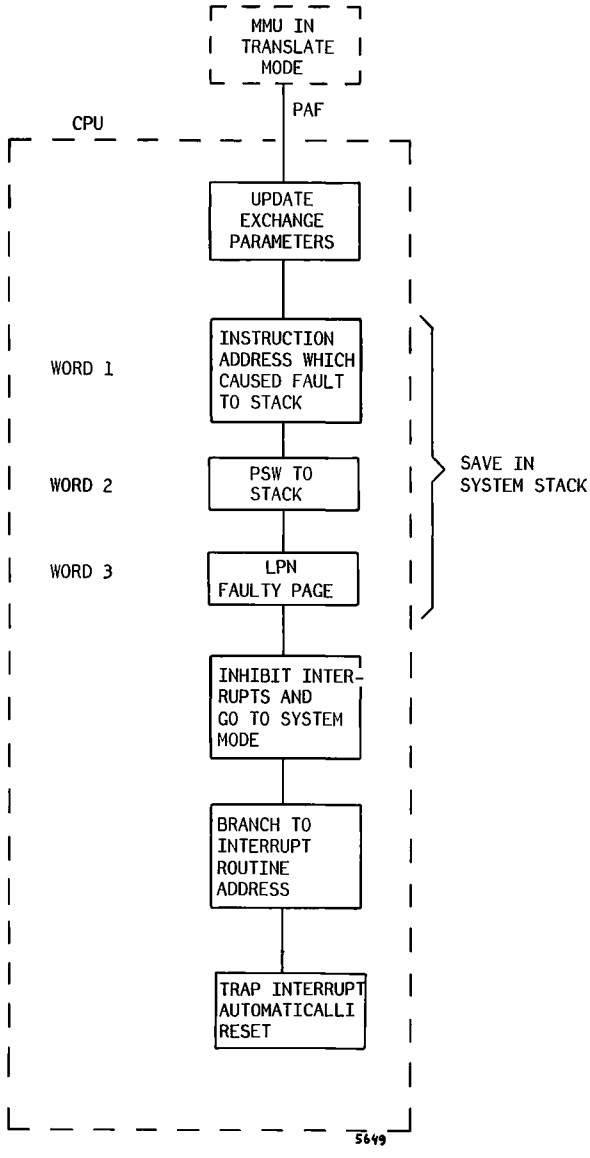


Figure 2.26 PAGE FAULT SEQUENCE

2.7.5 STOP ON PRESET ADDRESS (FIGURE 2.27)

The Stop On Preset Address (SOPA) Function, also known as Preset Access, enables the comparison between an address pre-loaded into a Register and the Memory Address Lines (MAD). Four facilities are available but the way in which these are inplemented depends on the Control Panel supplied with your system. see Figure 2.27. The four facilities are:

- Preset Access-Read or Write, for each Fetch - or Write Memory access a comparison is made between the Preset Address and MAD.
- Preset Access-Write Only, for each write memory access a comparison is made between the Preset Address and MAD.
- Preset Off, resets the address already loaded in the PRAD Register.
- Read Preset Address, reads the address from the MIOP Scratch-Pad.

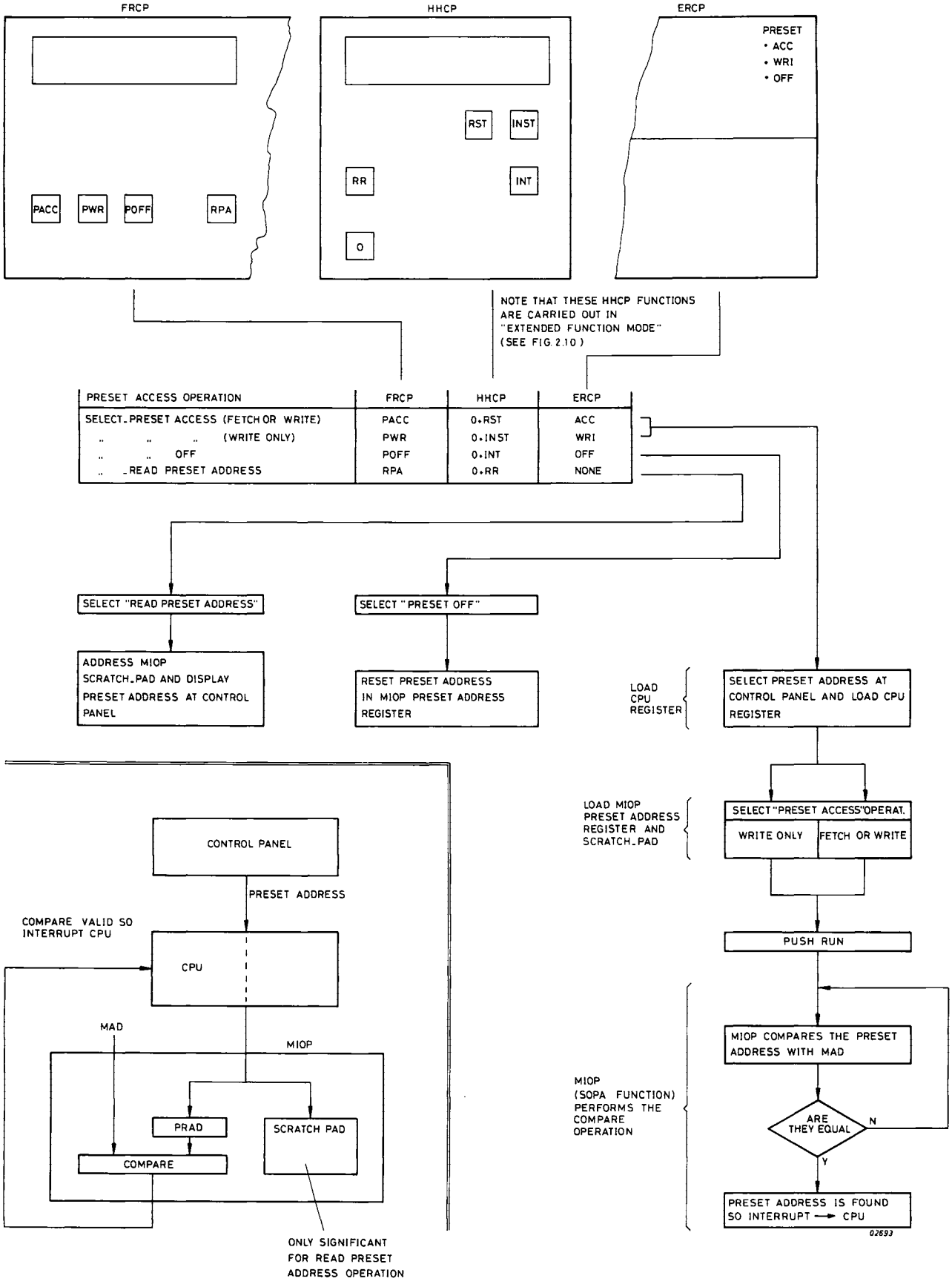


Figure 2.27 SOPA - PRINCIPLE OF OPERATION

3 DETAILED DESCRIPTION

LIST OF ILLUSTRATIONS

LIST OF TABLES

* Note: See section 3.19.2 for specification.

3.1 CPU ARCHITECTURE (FIGURE 3.1)

The basic P857E system configuration includes the following:

- Scratch Pad and Arithmetic Unit
- Logical Memory addressing up to 32k (16 bits) with CPU only
- Physical Memory addressing up to 8M words (24 bits) with the Memory Management Unit or 512K words (20 bits) via CPU with control panel LA function.
- Serial/parallel conversion (control panel and operator console)
- Machine state indicators
- IPL - 1K x 4 bit format.

3.1.1 SCRATCH PAD AND ARITHMETIC UNIT

The Scratch Pad and Arithmetic Unit is comprised of 4 LSI (Large Scale Integrated) circuits type 2901A. The 4 circuits are connected together for 16-bit operation in look-ahead carry mode. The principal logic elements of the 2901A are:

- Scratch Pad
- Source Selector
- Arithmetic Logic Unit
- Destination Selector
- Register Q

SCRATCH PAD

The Scratch Pad contains 16 registers A0-A15. The designation of these registers is as follows:

- A0 - scratch register.
- A1-A14 - these registers may hold one or both operands of an instruction or, a result. They may also be used as addressing or indexing registers with respect to memory.
- A15 - used as a stack pointer by the interrupt system. It may also be used in the same way as A1-A14.

SOURCE SELECTOR

The Source Selector forms a multiplexor input to the ALU. From the 5 operand sources micro-instruction bits enable the selection of 8 different combinations for input to ALU. These 8 combinations are selected by microinstruction bits 0, 1, 2.

ARITHMETIC LOGIC UNIT (ALU)

ALU receives the 2 x 16-bit operands and may perform up to 3 binary arithmetic functions or 5 logic functions on them. The 16-bit result is made available on the ALU lines. The 8 ALU functions are selected by micro-instruction bits 3, 4, 5.

DESTINATION SELECTOR

The Destination Selector forms a multiplexer input to the scratch pad and the Q register.
There are 8 possible combinations of destination for the output of the ALU, controlled by micro-instruction bit 6, 7, 8. The scratch pad can be loaded in 3 modes, which are: No shift, shift up and shift down.
Shifting can be done at the same time in register Q.
When shift up is done, the most significant bit of register Q is shifted out as an input to the selected scratch pad register, at the least significant side.
Shift down will result in shifting in the least significant scratchpad - bit into register Q at the most significant side.

REGISTER Q

Register Q is used for multiplication and division routines and also functions as an accumulator or holding register.

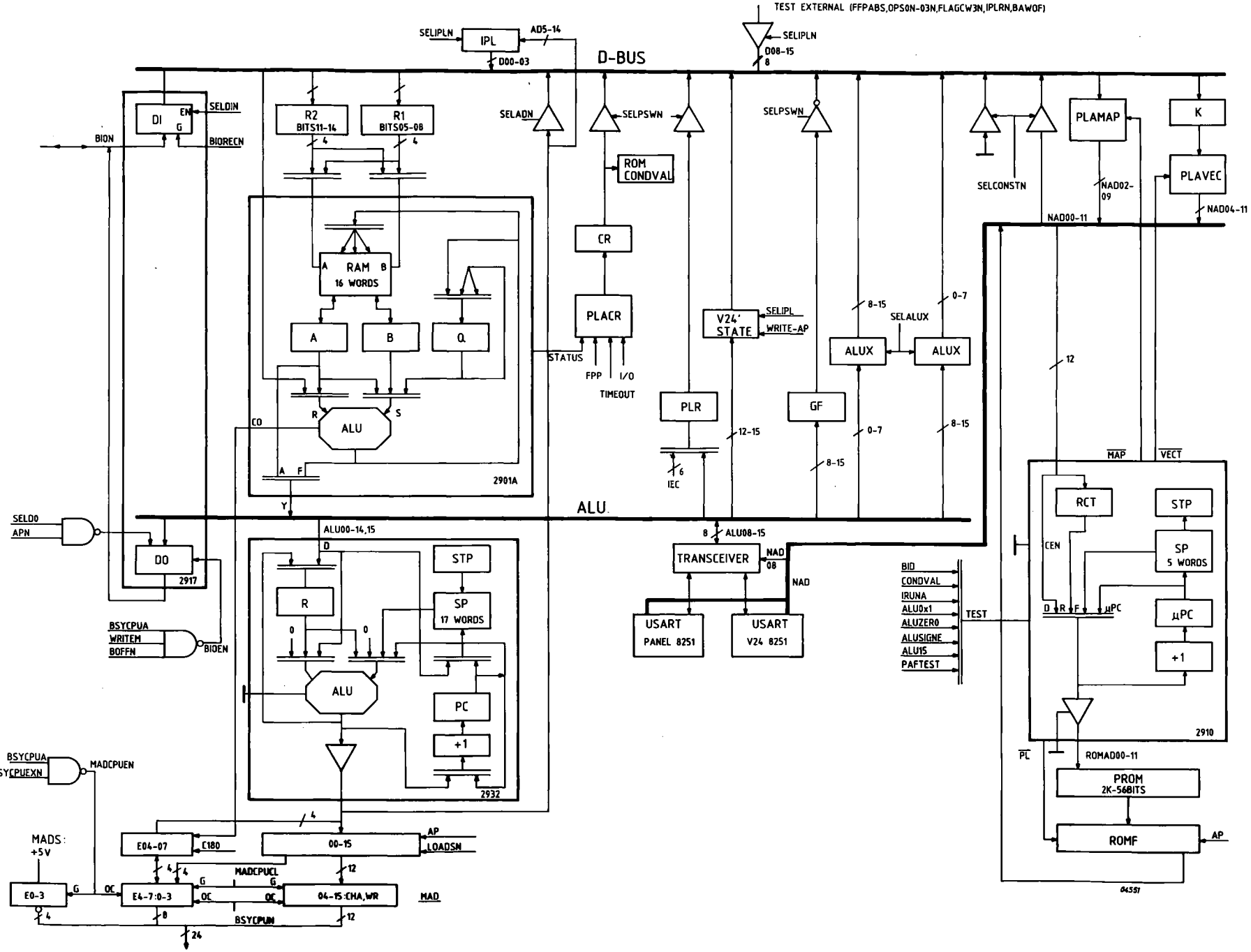


Figure 3.1 CPU ARCHITECTURE

3.1.2 MEMORY ADDRESSING

In the basic configuration the P857E employs 4 LSI circuits type 2932 connected for 16-bit operation in look-ahead carry mode. The principal logic elements of the 2932 are:

- LIFO Stack
- Auxiliary Register
- Program Counter
- Full Adder

LIFO STACK

The LIFO (Last In First Out) Memory Stack is 17 words deep to store subroutine return addresses.

AUXILIARY REGISTER

This is a holding register of either the output from the adder or from the ALU lines.

PROGRAM COUNTER

The Program Counter holds the current program address and at the end of every instruction it is incremented by 1. This is in fact A0 incremented by 2 each time.

FULL ADDER

The Full Adder operation is controlled by the micro-instructions. These micro-instructions select the appropriate multiplexor input at ports A and B. The result is either an address (MAD lines) or data for the internal bus (D lines). The Full Adder is only used in transparent mode.

3.1.3 MICROPROGRAM

The system microprogram is contained in 7 Programmable Read Only Memories (PROM) in the format 2,048 words x 56 bits. To access the instructions of this micro-program an 11-bit address is generated by a LSI circuit type 2910. The principal elements of the microprogram addressing are:

- Register K
- PLAVEC
- PLAMAP
- Microprogram Controller (2910)
- Microprogram PROMs
- ROMF which contains the micro-instruction currently being executed.

REGISTER K

Loaded from the system memory via the UPL Bus, the K register holds either the complete instruction or the most significant word of a double length instruction.

PLAVEC

PLAVEC is a Programmable Logic Array type 82S100 which forms a buffer stage between the K Register and 8 NAD (Next Address) Lines.

PLAMAP

PLAMAP is a Programmable Logic Array type 82S100 which senses the current state of the processor via its inputs. When one or more inputs are active a code is active at PLAMAP's output lines which form 8 of the NAD lines.

MICRO PROGRAM CONTROLLER

The Microprogram Controller is a LSI circuit type 2910, which takes its inputs from the NAD lines and via the ROMAD lines addresses the Microprogram PROMs. The principal logic elements of the 2910 are:

- Register Counter - loaded from the NAD lines it acts as a possible source for the next address.
- LIFO Stack - 5 word x 12-bit stack to provide return address linkage during subroutines or loops.
- Microprogram Counter - composed of a 12-bit incrementer followed by a 12-bit register.
- Instruction PLA - decodes the 16 micro-instructions which control internal chip operations.

MICROPROGRAM PROMS

The system Microprogram is contained in 7 PROMs in the format 2,048 words x 56 bits. The microprogram is addressed from the ROMAD lines enabling a 56 bit control micro-instruction to appear at the PROM outputs. This micro-instruction is an input to the ROMF Register.

ROMF REGISTER

This register contains the micro-instruction currently being executed.

3.1.4 SERIAL/PARALLEL CONVERSION

Serial to Parallel and Parallel to Serial conversion is carried out for the serial interfaces of P857E. A LSI circuit type USART is used for each interface. The interfaces are:

- control panel
- operators console

3.1.5 GENERAL F/FS

These are 8 F/Fs which indicate the following machine states: Run, Enable, Control Panel Interrupt, Power Failure, Real Time Clock, Program Interrupt, Extended Mode, User Mode. Some of these F/Fs receive their input from the ALU lines whereas some have direct condition inputs. All general F/Fs can be read from the D lines and the following are also read in the Program Status Word (PSW):

ENB - Enable (Bit 9)
FE - Extended Mode (Bit 13)
FU - User Mode (Bit 15)

PROGRAM STATUS WORD

The Program Status Word comprises the following: Program Level Register (PLR), the Condition Register (CR) and 3 of the General F/Fs already described above. The PSW is saved in the Stack during Call instructions, Interrupts or Traps and is restored with an RTN instruction.

3.1.6 ALUX

To exchange and store the value of ALU bits 0-7 to D08-15 and ALU 8-15 to D00-07 two ALUX Registers are employed. This operation is useful when performing operations such as exchange characters or load character as it reduces the CPU time involved.

3.2 SYSTEM CLOCKS (FIGURE 3.2)

The basic system clocks are derived from a crystal oscillator that drives a TTL divider network to generate 2 pulses:

- OSCA, a 45nS pulse for CPU timing (only generated if OSCENB is true).
- OSC, a 45nS pulse for MIOP timing.

3.2.1 CPU CLOCKS

The CPU clocks are shown in Figure 3.2 and comprise 3 basic counters.

- Timeout/Serial Counter, 2 outputs are used to give the serial interface cycle timing (SERCL) and the timeout clock pulse (TIMECL). This counter is continually counting.
- Timeout Counter, this counter is only clocked during a data transfer otherwise it is always held in the reset state.
- CPU Sequensor Counter, generates the necessary timing signals during the 4 CPU cycle types. The Sequensor is continually counting except for the cycle WAIT when it waits until the end of operation is indicated.

3.2.2 MIOP CLOCKS

The MIOP basic clock pulse of 90nS is derived from the CPU Clock and continually clocks the MIOP Sequensor. This Sequensor however, only starts if initiated for a Translate Cycle (MMU Function) or a Bus Request (IOP Function).

3.3 ARITHMETIC FUNCTION (FIGURE 3.3)

The Arithmetic Function of the P857E employs 4x 2901A ALU devices which generate a 16-bit address or operand at the ALU lines. For purposes of this description the Arithmetic Function is described in four parts:

- ALU (2901A) internal registers and control.
- external shift control logic.
- address and operand generation.
- ALU operations.

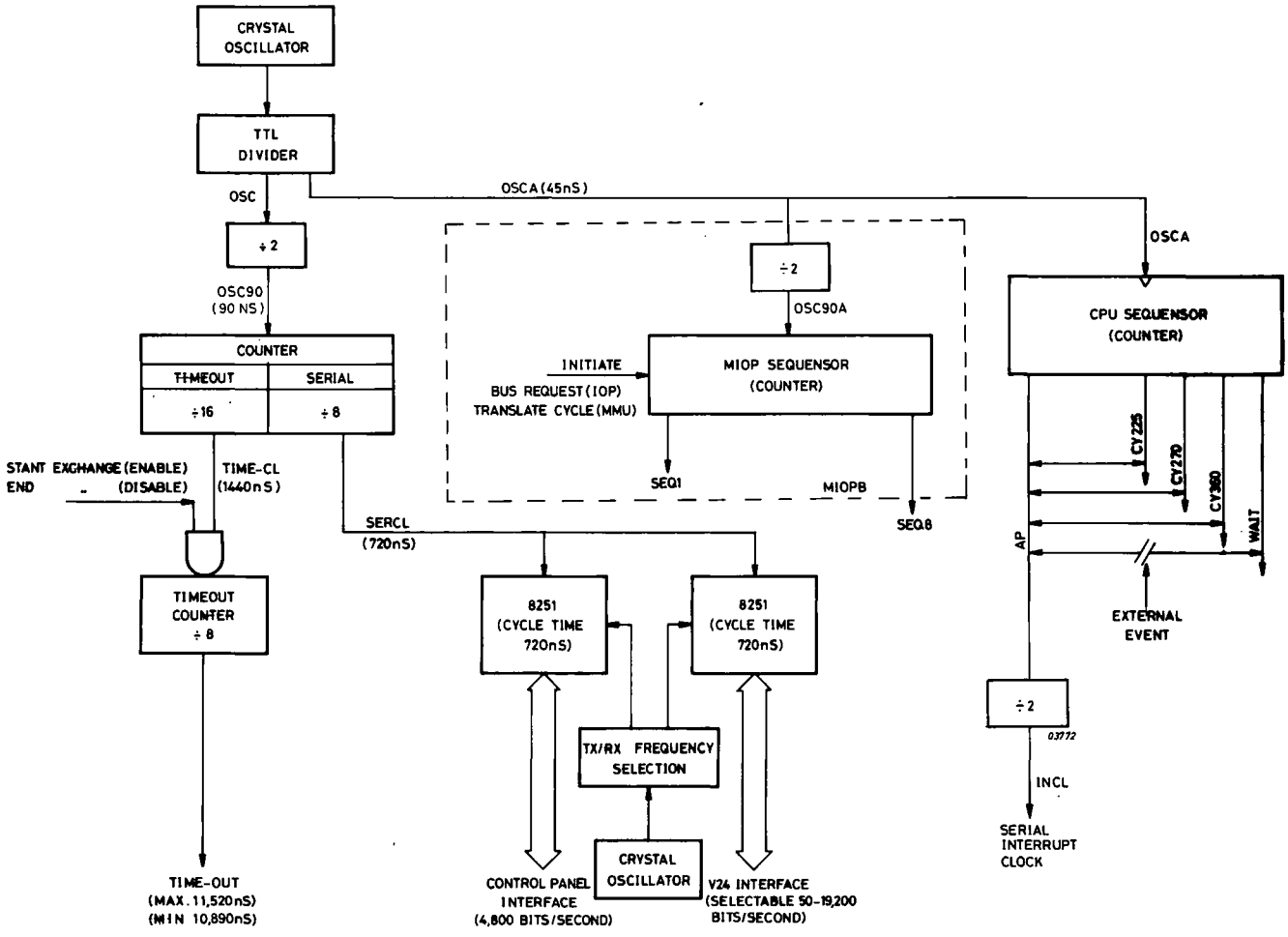


Figure 3.2 P857E SYSTEM CLOCKS

3.3.1 ALU

There are 4 ALU devices connected for 16-bit operation, the principal registers being the Scratch Pad (or RAM), Register Q, Source Selector and the 8-function ALU.

SCRATCH PAD

The Scratch Pad is a 16x16 bit RAM which may be addressed by 2 external ports A and B.

- For read operations ports A and B are used.
- For write operations only port B is used.

Note that the register addressed by port A may be enabled directly at the output. The A and B ports enable the addressing of the 16 registers contained in the Scratch Pad. The input to these ports is via the ALUA and ALUB lines which contain either the R1 field content (D5, D6, D7, D8), or the R2 field content (D11, D12, D13, D14).
Note that the register addressed by port A can only be read and not written.

SOURCE SELECTION

The ALU source code (bits 0, 1, 2) select one pair of source operands. The source operands available are D, A, B, Ø, Q of which 8 combinations are used:
AQ, AB, ØQ, ØB, ØA, DA, DQ, DØ.

EIGHT-FUNCTION ALU

The 8-function ALU receives 2 operands at R and S and can perform 3 binary and 5 logic operations.

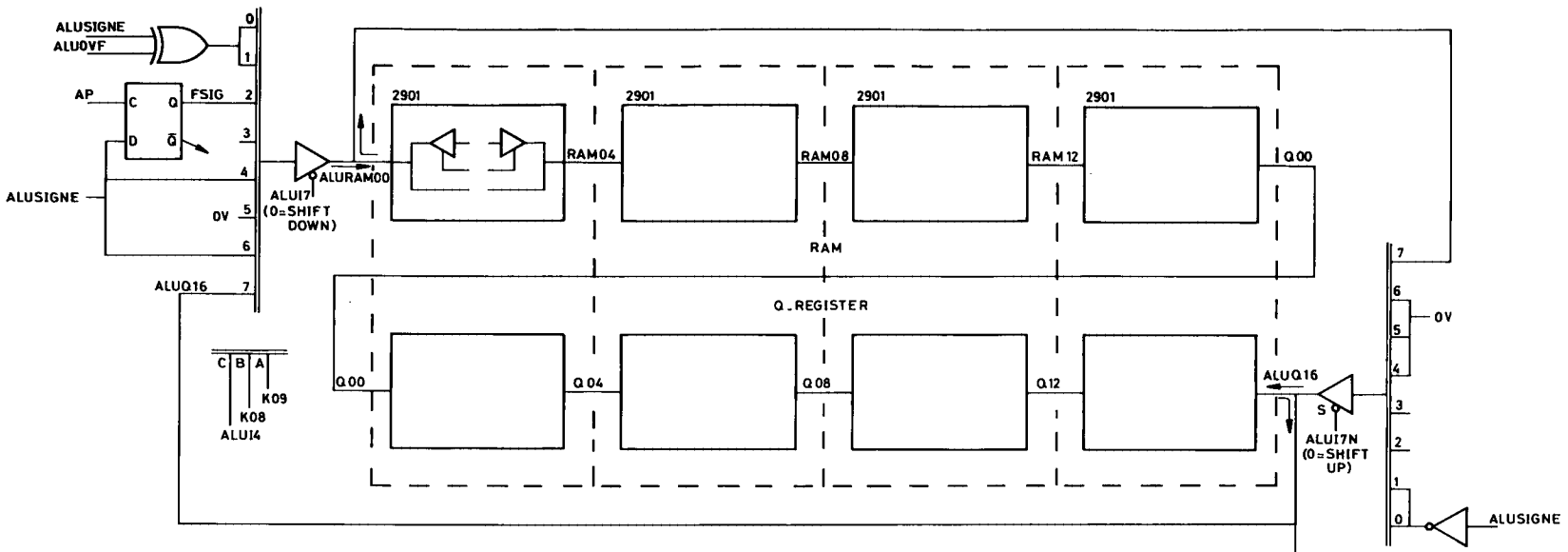
3.3.2 EXTERNAL SHIFT CONTROL LOGIC (FIGURE 3.3A)

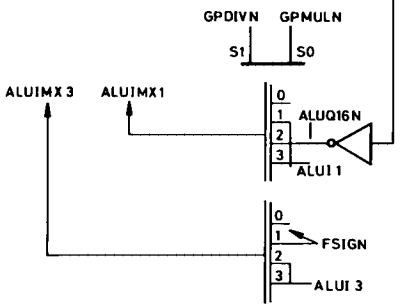
The shift control logic is shown in a simplified form in Figure 3.3A. Three multiplexors are responsible for this control.
The shift-left and shift-right multiplexors one of which is enabled depending on the value of Micro-Program signal ALUI7 and the appropriate input is selected by a code on the lines ALUI4, K08, K09 (see Tables of 3.3A).
The third multiplexor enables 2 signals ALUIMX1 and ALUIMX3 which form a part of the 9-bit micro-instruction for the 2901 (see Table of 3.3A).
Two examples of this shifting are given in figure 3.3A: Instruction SRC and SLA.

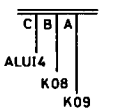
3.3.3 ADDRESS AND OPERAND GENERATION

The generation of a 16-bit address or operand (without shift logic) is shown in Figure 3.3B. Data is written from the D lines into either R1 or R2 registers (R1 and R2 of the instruction field) which can then address either ports A or B via the ALUA or ALUB Multiplexors.

The Look-ahead Carry facility is a carry look ahead generator type 74S182 which samples the Carry and Propagate outputs of the ALU 0, 1 and 2 to enable the appropriate Carry Enable for ALU 1, 2 and 3.







LS251

C	B	A		
ALUI4	K08	K09	ALURAM00	
0	0	0	OVFØSIG	MULTI
0	0	1	OVFØSIG	MULTI
0	1	0	FSIG	SLN,DLN
0	1	1		
1	0	0	ALUSIGNE	SRA,DRA
1	0	1	OV	SRL,DRL
1	1	0	ALUSIGNE	SRN,DRN
1	1	1	ALUQ16	SRC,SRC

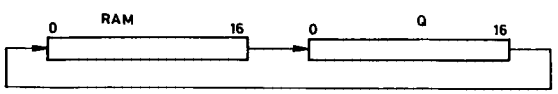
S153

S1	S0	2901 SRC	290 LOPER
GPDIVN	GPMULN	ALUIMX1	ALUIMX 3
0	0		
0	1	ALUI 1	FSIGN
1	0	ALUQ16N	ALUI3
1	1	ALUI 1	ALUI3

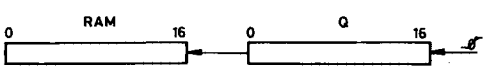
C	B	A		
ALUI4	K08	K09	ALUQ16	
0	0	0	ALUSIGNEN	DIVI
0	0	1	ALUSIGNEN	DIVI
0	1	0		
0	1	1		
1	0	0	OV	SLA,DLA
1	0	1	OV	SLL,DLL
1	1	0	OV	SLN,DLN
1	1	1	ALURAM00	SLC,DLC

03546

EXAMPLE: SRC K08=1 K09=1
ROM: ALUI4 = 1
ALUI7 = 0



EXAMPLE: SLA K08=0, K09=0
ROM: ALUI4=1
ALUI7=1



SHIFT LOGIC

FIGURE 3.3A ALU SHIFT CONTROL LOGIC

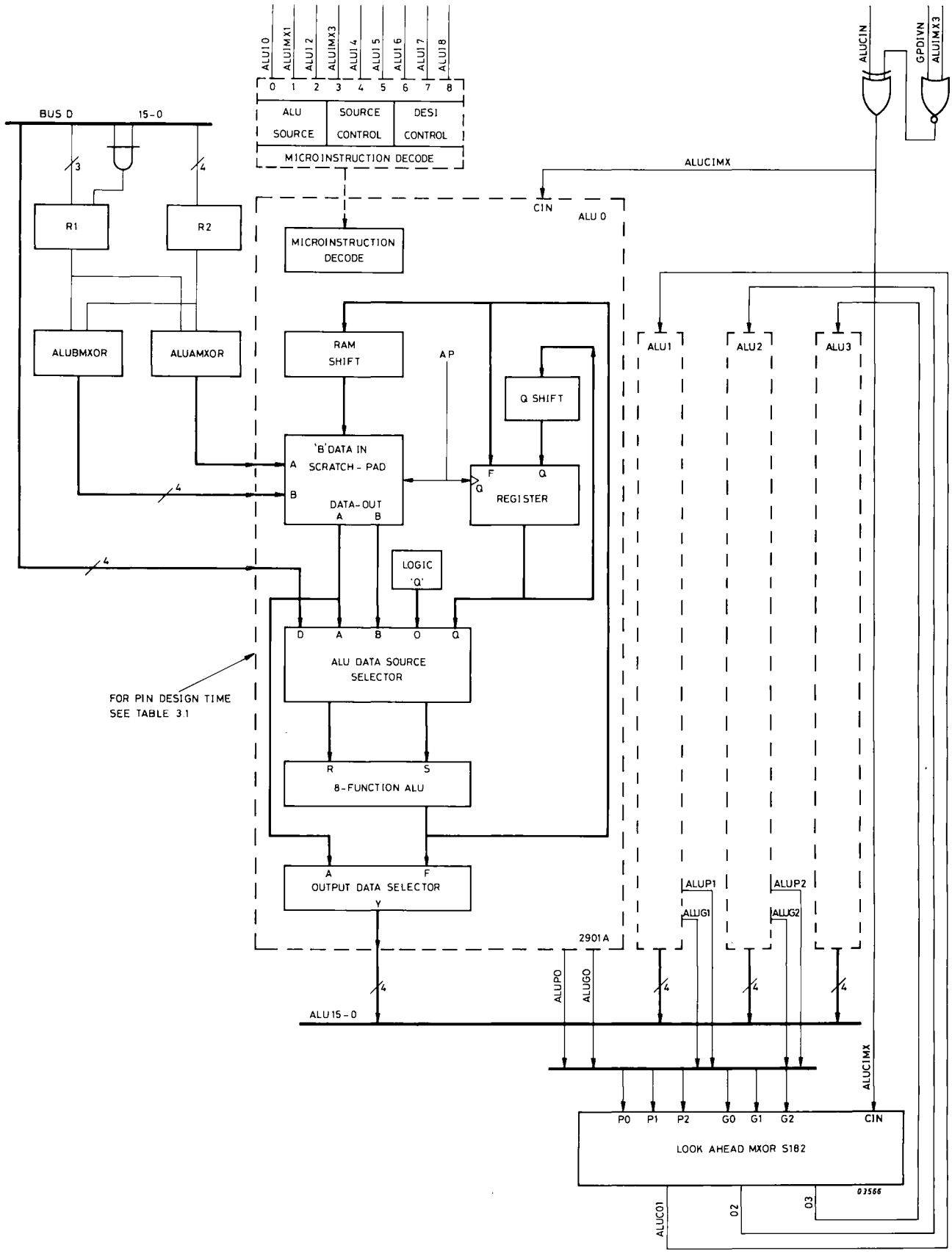
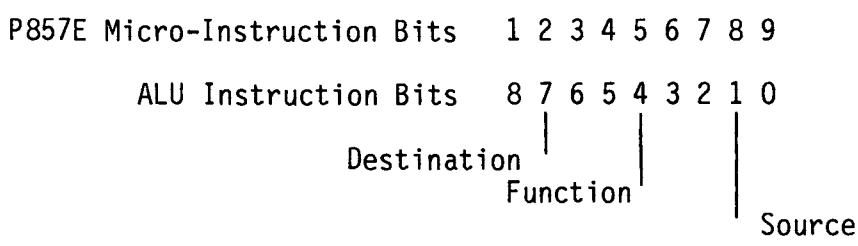


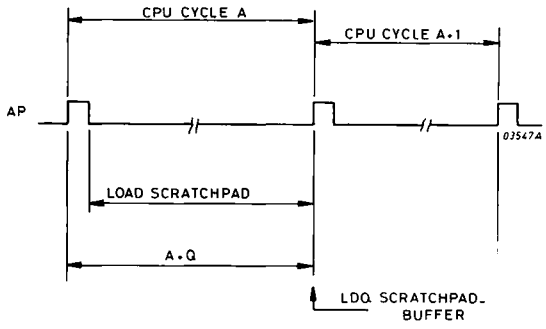
Figure 3.3B LOOK-AHEAD CARRY AND ALU 00-15 CONFIGURATION

3.3.4 ALU OPERATIONS

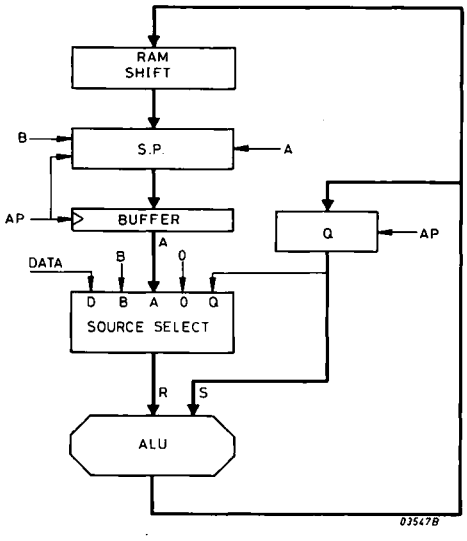
The arithmetic operations of ALU are under control of bits 1-9 of the Micro-instruction currently being executed. These bits correspond to the ALU bits as follows:



Two examples of Scratch Pad and Q Register shift operations are given in Figure 3.3A and 2901 operations at P857E level is shown in Figures 3.3C and 3.3D.

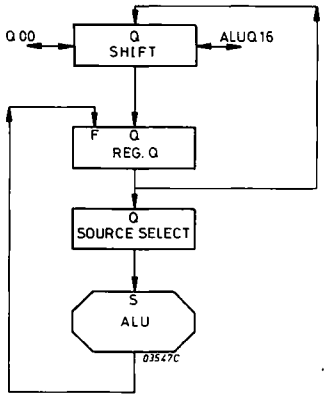


Both the Scratch Pad buffer and Q Register are constantly clocked by AP. Q is loaded at the leading edge of the AP puls in the next cycle after the ALU operation (A+Q).
The scratch pad is loaded during the time that AP is low.



Updating the Scratch Register

The Scratch Register addressed by Port B receives data from the ALU using the data path shown.
The ALU output is also loaded in Q at AP.
ALU = Q + A
(A = content of scratch pad reg. addressed by port A).
Write in Register pointed by Port B.



Register Q

Used principally for multiplication and division but also for storage. The Q Register is in effect a multiplexer to enable:
. Loading the ALU output
. Shifting the content of Q left or rigth.

Figure 3.3C SCRATCH PAD AND Q REGISTER OPERATIONS

Pin No.	2901A Name	P857 Name	Description
4	A0	ALUA0)	Port A of the Scratch Pad for read operations only,
3	A1	1)	loaded from the R1 or R2 instruction fields.
2	A2	2)	
1	A3	3)	
17	B0	ALUB0)	Port B of the Scratch Pad for read or write opera-
18	B1	1)	tions, loaded from the R1 or R2 instruction fields.
19	B2	2)	
20	B3	3)	
25	D0	)	This is the data input from the Bus D (see C7E1/A for
24	D1	)	the P857 signal name) which can be selected as one of
23	D2	)	the ALU data sources, D0 is the least significant bit.
22	D3	)	
40	$\overline{OE}$	SEL2901N	This is the ALU output enable active low, when high the outputs are off.
21	Q0	)	These are the shift lines of the lsb of the Reg. Q
		)	and RAM.
9	RAM0	)	
36	Y0	)	This is the data output (3-state), (see C7E1/A for the
37	Y1	)	P857 signal name) which displays either the ALU output
38	Y2	)	or the data on Port A.
39	Y3	)	
35	$\overline{P}$	)	The Carry and Propagate outputs for the Look-ahead
		)	Carry logic (see C7E1/A for the P857 signal name).
32	$\overline{G}$	)	
11	F=0	ALUZERO	Output to indicate that the result of ALU operation is zero.
8	RAM3	)	These are shift lines of the most significant bit of
		)	the Reg Q and RAM.
16	Q3	)	
33	Cn+4	ALUMADP1	The carry output of the msb.
34	OVR	ALUOVF	The result of an arithmetic 2's comp. has overflowed into the sign-bit.
31	F3	ALUSIGNE	The most significant bit of the ALU output.
12	I0	ALUI0)	These 9 instruction lines indicate data source I0, 1,
13	I1	ALUIMX1)	2) function (I3, 4, 5) destination (I6, 7, 8).
14	I2	ALUI2)	Seven of these lines are from the Micro-Program and
26	I3	ALUIMX3)	two lines MX1 and MX2 are from a multiplexor for
28	I4	ALUI4)	shiftoperations (see table inset in Figure 3.3A).
27	I5	5)	
5	I6	6)	
7	I7	7)	
6	I8	8)	
29	Cn		Carry input for the Look-ahead Carry Logic (see C7E1/A for the signal name).
15	CP	APA	Indicates the beginning of a CPU cycle, the RAM and Q outputs change on the low to high transition.

Table 3.1 2901A PIN DESIGNATIONS

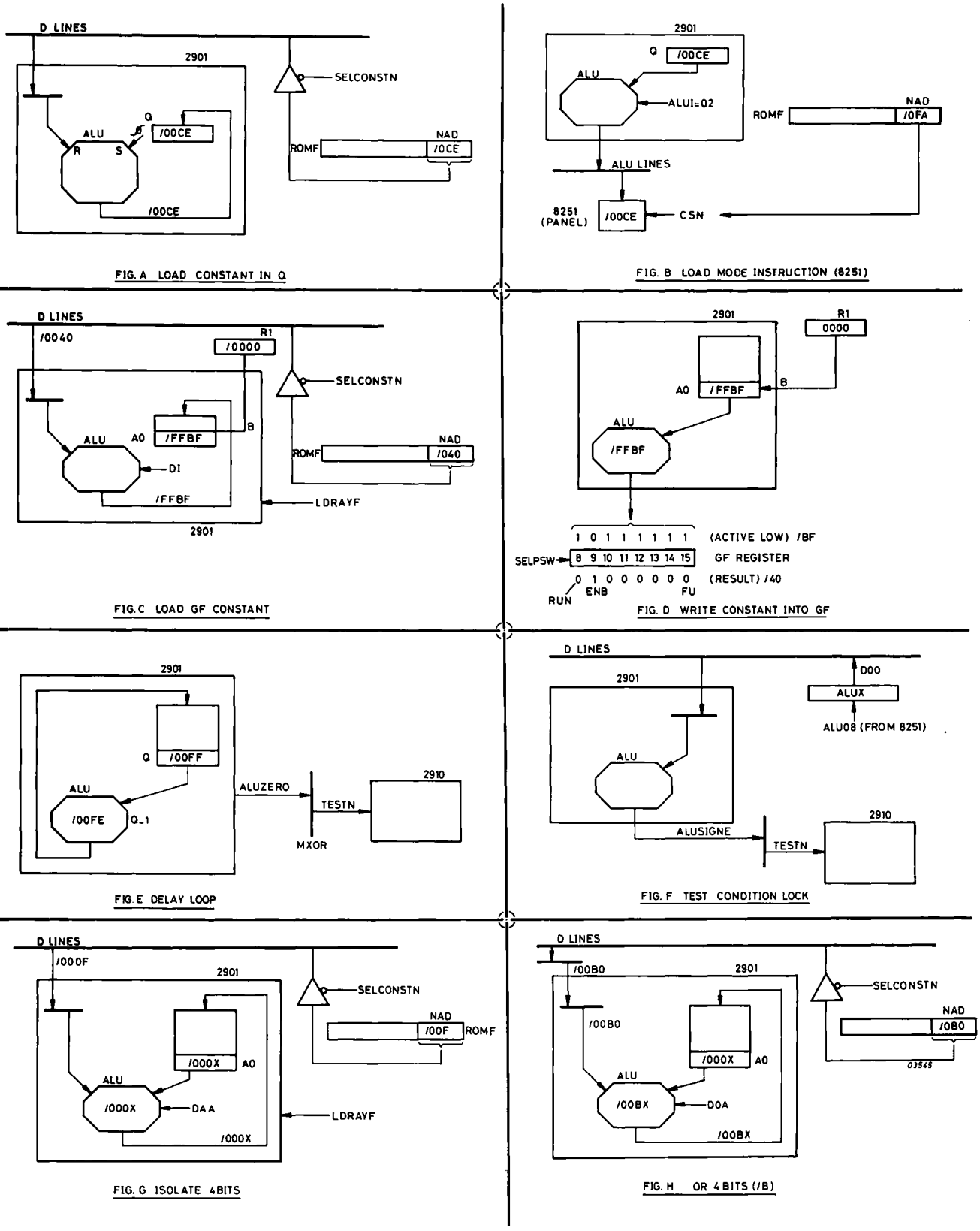


Figure 3.3D 2901 OPERATIONS

3.4 MEMORY ADDRESSING (FIGURE 3.4)

For Memory addressing the P857E employs an address sequensor and associated Buffer Logic on the card C7E2B. Diagram C7E2/B shows the interfaces which affect the Memory Address functions in the CPU and diagram MIOP/D shows the MIOP - Memory Address Function.

3.4.1 ADDRESS SEQUENSOR (TYPE 2932, FIGURE 3.1)

The P857E employs 4x 2932 devices to generate the 16 address bits either to load MADS or to load the D lines for 2901. The principal features are:

- Adder with input multiplexors.
- Program Counter Register with an incrementer and input multiplexor.
- A 17x4 Last-In, First-Out Stack consisting of an input multiplexor, a 17x4 RAM and a Stack pointer.
- An Auxiliary Register with input multiplexor.
- An Instruction Decoder for 16 micro-instructions of which 12 are used by the P857E.
- Four 3-state output buffers at the address outputs.

ADDER

The Adder is a binary device with full look-ahead carry logic for high speed addition. The carry output from one device is connected to the next higher carry input. When an addition is not performed the carry input is internally inhibited and data passes directly through the Adder. The multiplexors at the A and B inputs are selected by the micro-instruction. The P857E uses this adder in transparent mode only.

PROGRAM COUNTER

The Program Counter Register (PC) is loaded from the Incrementer on the low to high transition of the clock pulse at the end of every instruction. The carry output from the incrementer is connected to the next higher carry input. For reasons of performance the real value of the Program Counter is always PC + 4; e.g. when addressing /100 the value of PC is /104.
The least significant bit is at CP7EB level used as the least significant bit but one (see diagram CP7RA/I).
In this way addition "+1" results in "+2" of the Program Counter.

LIFO STACK

The LIFO (Last In First Out) Stack consists of a multiplexor, a 17x4 RAM and a Stack Pointer (SP) to address the words in the RAM. The SP always points to the last word written into the RAM (top of the Stack) which is available at the output. Data is pushed onto the top of the Stack (DI) from either D or PC and written into location SP + 1. The SP is decremented on the low to high transition a the end of the cycle so that it still points to the last data written into the RAM. The Stack Pointer is decremented for POPS (Pop Stack) and RTS (Return Stack). It is incremented and loaded for instructions PSHD (Push D), PSHP (Push PC) and JSBR (Jump Subroutine). Note that the Stack is also useful in extending the 2901 capacity of working registers.

AUXILIARY REGISTER

The Auxiliary Register (R) is loaded from either the D input or from the Adder. If specified in the micro-instruction then it is loaded on the low to high transition of the clock output.

INSTRUCTION DECODER

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP and RAM.

OUTPUT BUFFERS

The Address Outputs are 3-state drivers which may be disabled by the micro-instruction.

MICRO-INSTRUCTION SUMMARY

The P857E employs the following micro-instructions.

Instruction Number	I_3	I_2	I_1	I_0	Mnemonic	Instruction	Y_0-Y_3	Next State (after CP) PC	R	RAM	SP	Note
0	L	L	L	L	PRST	RESET	"0"	"0"+C_i	-	-	Reset	
1*	L	L	L	H	PSUS	SUSPEND	Z(Note 1)	-	-	-	-	
2	L	L	H	L	PSHD	PUSH D	PC	PC+C_i	-	D to Loc SP+1	SP+1	
3	L	L	H	H	POPS	POP S	S	PC+C_i	-	-	SP-1	
4	L	H	L	L	FPC	FETCH PC	PC	PC+C_i	-	-	-	
5	L	H	L	H	JMPD	JUMP D	D	D+C_i	-	-	-	
6	L	H	H	L	PSHP	PUSH PC	PC	PC+C_i	-	PC to Loc SP+1	SP+1	
7	L	H	H	H	RTS	RETURN S	S	S+C_i	-	-	SP-1	
8	H	L	L	L	FR	FETCH R	R	PC+C_i	-	-	-	
9*	H	L	L	H	FPR	FETCH PC+R	PC+R+C_n	PC+C_i	-	-	-	
10	H	L	H	L	FPLR	FETCH PC to R	PC	PC+C_i	PC	-	-	
11	H	L	H	H	JMPR	JUMP R	R	R+C_i	-	-	-	
12*	H	H	L	L	JPPR	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	-	-	-	
13	H	H	L	H	JSBR	JSB R	R	R+C_i	-	PC to Loc SP+1	SP+1	
14*	H	H	H	L	JSPR	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	-	PC to Loc SP+1	SP+1	
15	H	H	H	H	PLDR	LOAD R	PC	PC+C_i	D	-	-	

PC - Program Counter SP - Stack Pointer
R - Auxiliary Register D - Direct Inputs

Notes: 1. Z = High impedance state (outputs "OFF")
2. - = No change
* = Not used.

Table 3.2 2932 MICRO-INSTRUCTIONS

3.4.2 2932 OPERATIONS (FIGURE 3.4)

The 2932 is principally used to enable a 16-bit format (address or data) from the ALU lines to the AD lines. An example of some 2932 operations is given in Figure 3.4.

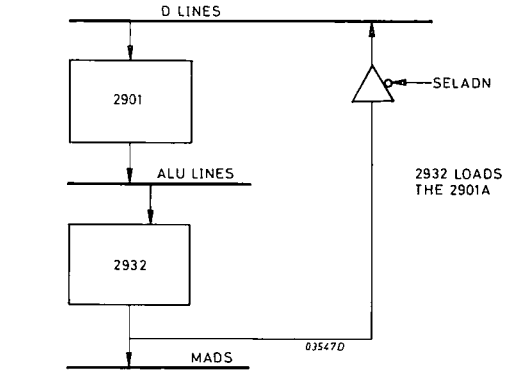
Pin No.	2932 Name	P857 Name	Description
1	I0	PCI0)	
19	I1	1)	Micro-instruction inputs which are decoded to control the
18	I2	2)	2932 internal functions.
17	I3	3)	
6	Y0	ADXX)	
7	Y1	XX)	3-state outputs from the 2932 to form the AD lines.
8	Y2	XX)	
9	Y3	XX)	
16	D0	ALUXX)	
15	D1	XX)	Data inputs from the Arithmetic Logic Unit (2901A).
14	D2	XX)	
13	D3	XX)	
2	$\overline{\text{FULL}}$		Not used.
3	Ci	PCCIX	Carry input from a lower device to externally increment the PC.
4	Ci+4	PCCIX	Carry output to a higher device to externally increment the PC.
5	Cn	PCCNX	Look ahead carry from the lower device to provide ripple block arithmetic.
12	Cn+4	PCCNX	Look ahead carry to a higher device to provide ripple block arithmetic.
11	CP	APB	System Clock Pulse.

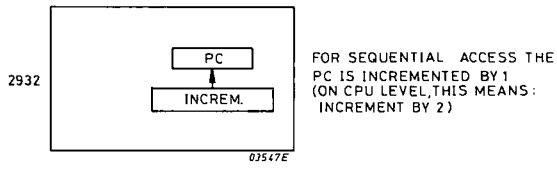
Table 3.3 2932 PIN DESIGNATIONS

3.4.3 DOUBLE BUFFERING MAD (SEE ALSO CHAPTER 3.8.4)

For speed reasons a double buffering of MAD is implemented in the P857E (see figure 3.1). This enables the CPU to prepare already the next address in the first MAD buffer when the second buffer still contains the current address (SLAVE to MASTER EXCHANGE only).

For MASTER to SLAVE EXCHANGE the CPU must wait until a complete cycle (see chapter 2.5) is finished because there is no double buffering for the BION lines.





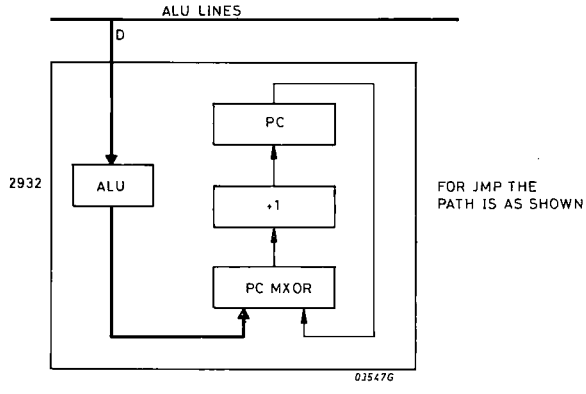


Figure 3.4 2932 OPERATIONS

3.5 MICROPROGRAM ADDRESSING (FIGURE 3.5)

The Microprogram Addressing logic of the P857E is shown in Figure C7E1/B and has the following structure:

- Microprogram Controller type 2910 which controls the addressing and execution of the micro-instructions contained in the Microprogram PROMs.
- The Microprogram is contained in 7 PROMs type 82S191 which store the microprogram in a 2,048 word x 56-bit format.
- ROMF Registers contain the 56-bit micro-instruction currently being executed.
- Next Address Generators, there are 3 ways of generating a new address: PLAMAP which is a Programmable Logic Array and senses the machine states, PLAVEC which is a Programmable Logic Array and takes the instruction format from Register K as its input.
  The Next Address Field of the micro-instruction currently being executed (explicit address).
- Test External Result.
  The CONDVAL multiplexor tests for the Branch instructions and its output CONDVAL is one of the inputs for the TEST multiplexor which tests different machine conditions and indicates the result to the 2910 with signal TESTN.

3.5.1 MICROPROGRAM CONTROL (2910)

The 2910 is used by the P857E to control the execution sequence of the microprogram stored in the PROM. The 2910 enables sequential access and also the possibility of branching to different parts of the microprogram. The 2910 receives 12 NAD (Next Address) lines and transmits 11 ROMAD (ROM Address) lines to address the microprogram words under control of the ROMADIO-3 lines (2910 instruction). The principle registers of the 2910 are the LIFO Stack, Register Counter (RCT), Microprogram Counter, Micro-instruction Decoder.

LIFO STACK

This Stack type LIFO (Last In First Out) can store 12-bit words up to 5 words deep. This enables the 2910 to jump to a sub-routine (Micro-inst CJS) and then return to the original routine (Micro-inst CRTN).

REGISTER COUNTER

This is a pre-settable down counter which is loaded with a value /XXX (ROMADLDN = 0) enabling instructions to be repeated or as a delay whereby the 2910 stays in a loop for a maximum count of /FFF. These functions are executed with either the RFCT or RPCT micro-instructions.

MICROPROGRAM COUNTER

For every micro-instruction the Microprogram Counter (Micro-PC) provides a 12-bit address from one of 4 sources:

- Micro-Program Address Register which usually contains the value of previous address + 1.
- A direct input from the NAD lines.
- The content of the Register Counter.
- A word from the LIFO Stack.

MICRO-INSTRUCTION DECODER

The Input to the 2910 micro-instruction decoder is given by bits ROMADI 0-3. When decoded these lines represent 16 instructions which control the flow of data in the 2910 and also select the source for the NAD lines. Only instructions 2 and 6 select PLAMAP and PLAVEC respectively otherwise the Branch Address is used. A summary of the instructions follows in Table 3.4 and their significance is shown in Figures 3.5A to 3.5E.

Hex. Code	Inst. Name	Description
0	JZ	Jump to Zero
1	CJS	Conditional Jump to Subroutine, Pipeline
2	JMAP	Jump MAP
3	CJP	Conditional Jump to Pipeline
4	PUSH	PUSH/Conditional, Load Counter (used together with 8)
5*	JSRP	Conditional Jump to Subroutine, Reg/Counter or Pipeline
6	CJV	Conditional Jump Vector
7*	JRP	Conditional Jump, Reg/Counter or Pipeline
8	RFCT	Repeat Loop, CNTR=0
9	RPCT	Repeat Pipeline, CNTR=0
A	CRTN	Conditional Return
B	CJPP	Conditional Jump Pipeline and POP
C	LDCT	Load Counter and continue (used together with 9)
D	LOOP	Test End Loop
E	CONT	Continue
F	TWB	Three-way branch

* Not used.

Table 3.4 2910 MICRO-INSTRUCTIONS

3.5.2 MICROPROGRAM

The system microprogram is contained in a 56-bit format subdivided into fields, each field controlling one or more functions. The 56-bit word is shown in Table 3.6 and a brief description of each mnemonic is given in Table 3.7.

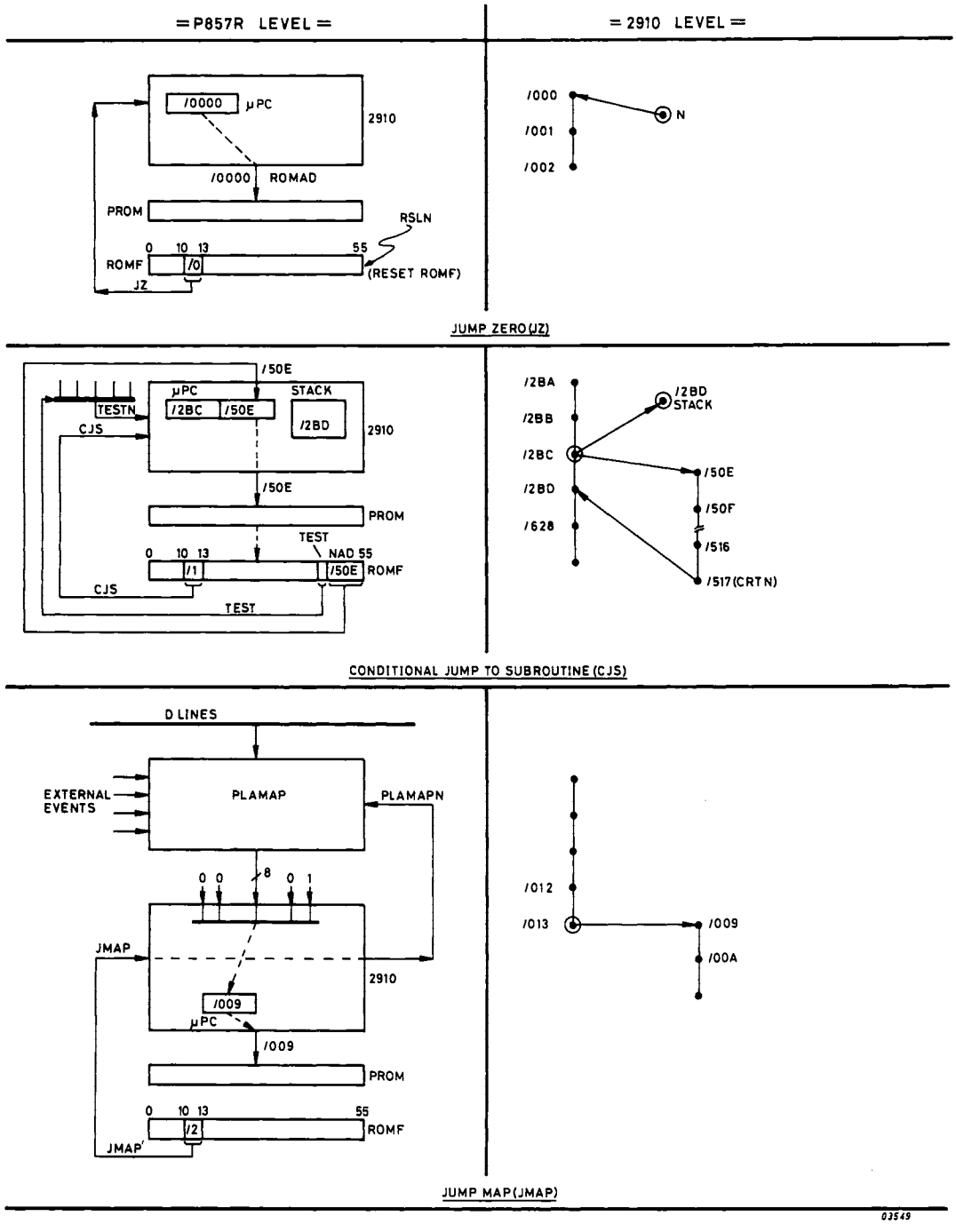


Figure 3.5A 2910 ROUTINES - JZ, CJS, JMAP

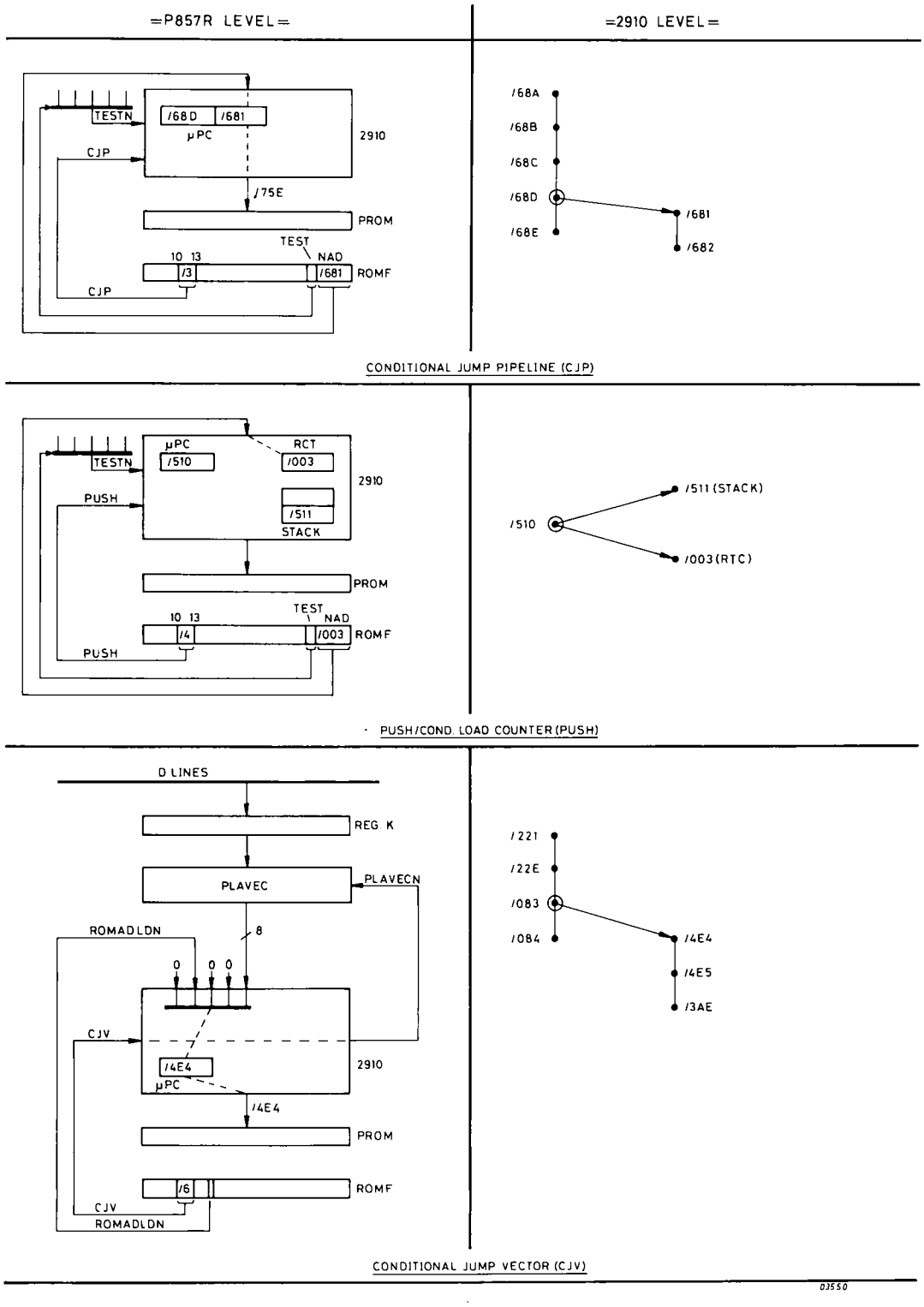


Figure 3.5B 2910 ROUTINES - CJP, PUSH, CJV

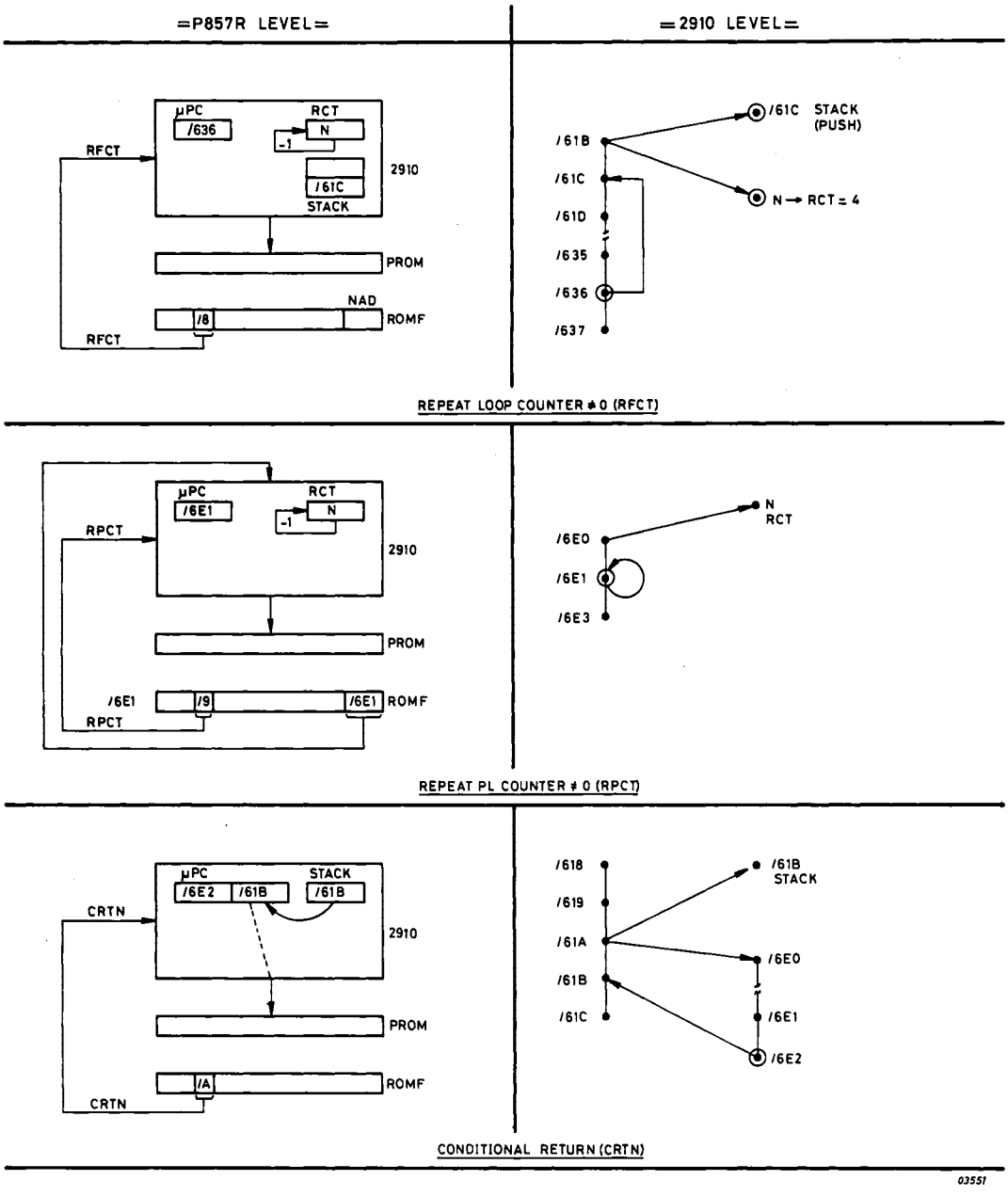


Figure 3.5C 2910 ROUTINES - RFCT, RPCT, CRTN

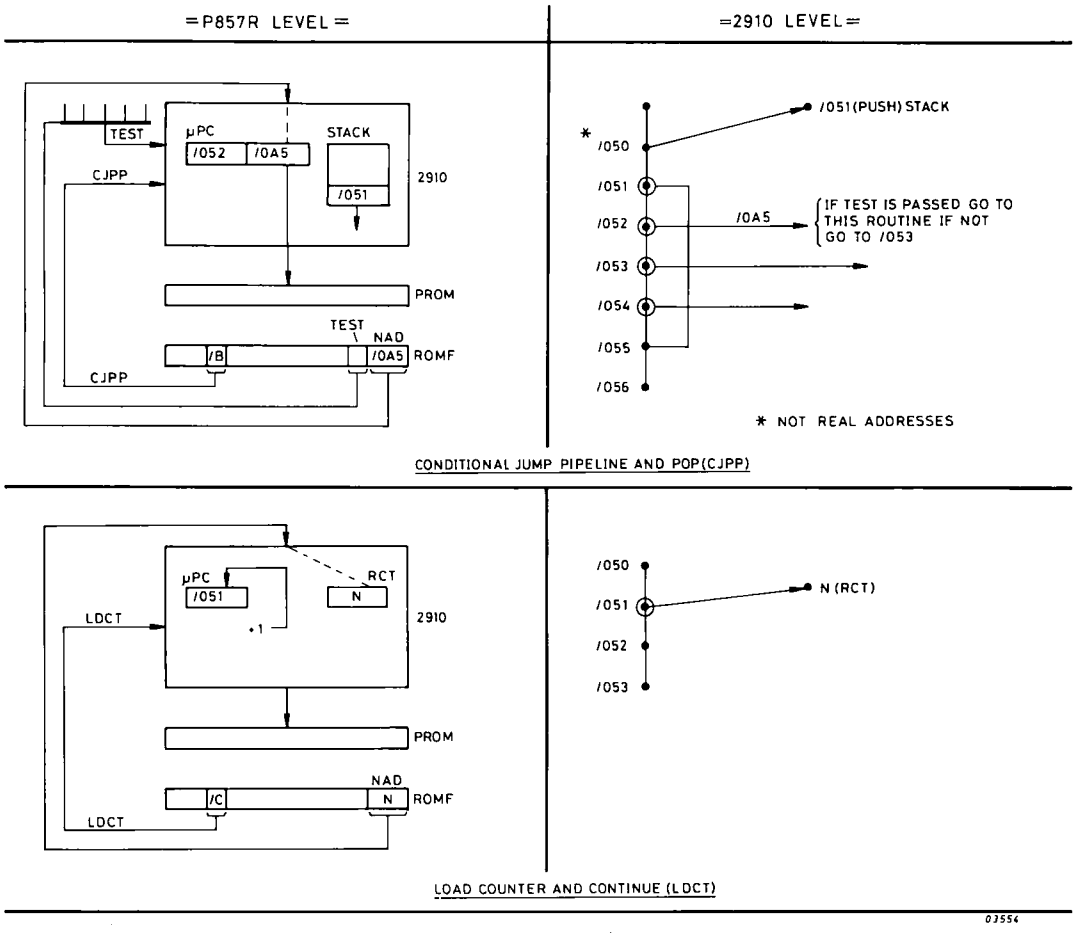


Figure 3.5D 2910 ROUTINES - CJPP, LDCT

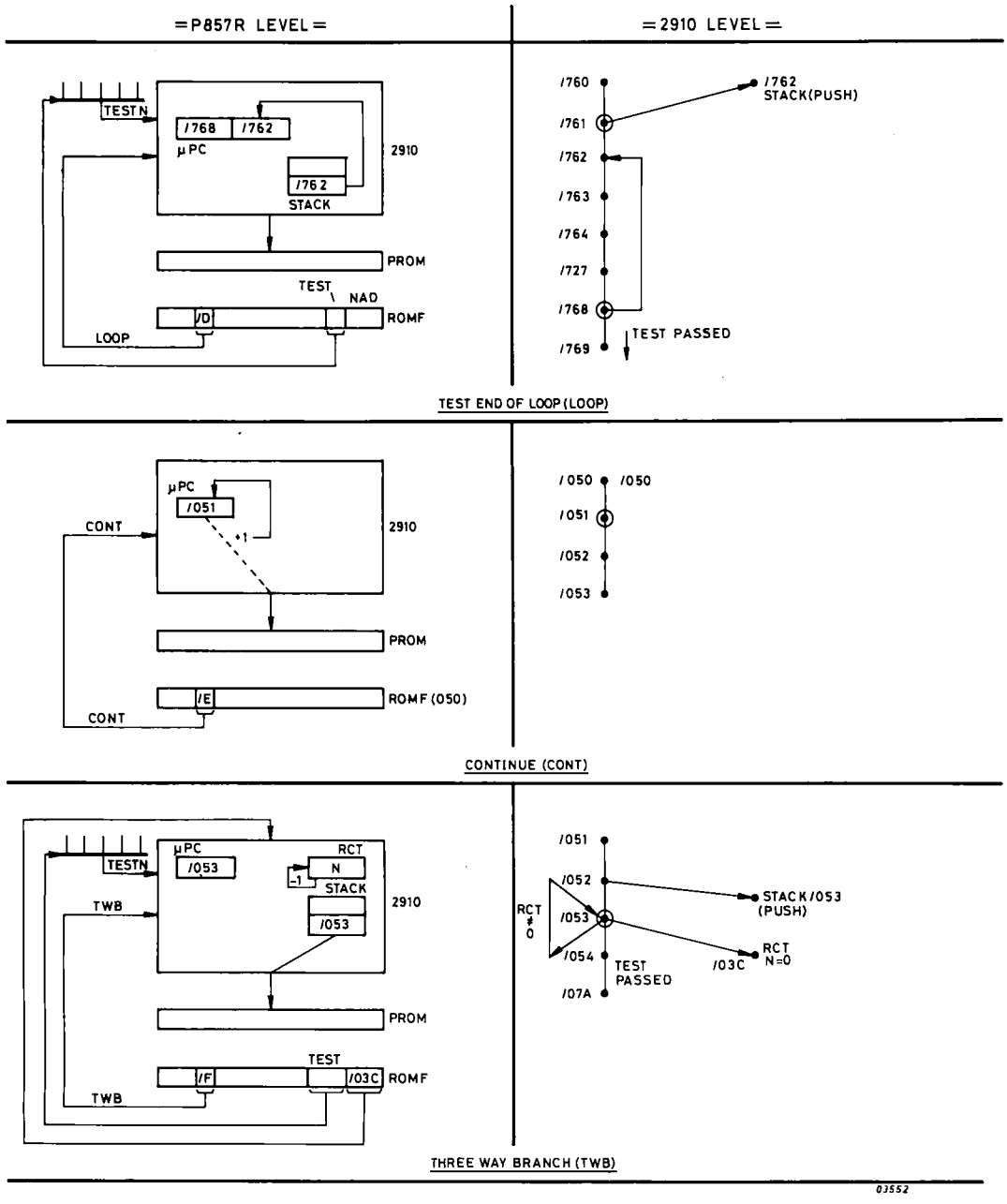


Figure 3.5E 2910 ROUTINES - TEST, CONT, TWB

Pin No.	2910 Name	P857 Name	Description
34	D0	NAD11	Next Address lines are the 2910 data inputs from either PLAMAP, PLAVEC or NAD. NAD11 is least sig. bit
36	D1	10	
38	D2	09	
40	D3	08	
02	D4	07	
04	D5	06	
17	D6	05	
19	D7	04	
21	D8	03	
23	D9	02	
25	D10	01	
27	D11	00	
08	I3	ROMADI3	Micro-instruction decode lines are decoded for the 2910 internal control signals and also select the source input for the NAD lines.
09	I2	2	
11	I1	1	
12	I0	0	
15	RLD	ROMADLDN	When low forces the loading of the Reg/Counter regardless of instruction.
31	CP	AP	Clock pulse triggers all internal changes on the low to high edge.
14	CCN	TESTN	Low indicates that the test is passed, this signal represents several P857E tests (see Table 3.10).
13	CEN	OV	
29	OEN	ROMADEN	Held permanently low to permanently enable the Y outputs.
33	Y0	ROMAD10	Address lines to the Microprogram PROMs. ROMAD10 is least sig. bit.
35	Y1	09	
37	Y2	08	
39	Y3	07	
01	Y4	06	
03	Y5	05	
18	Y6	04	
20	Y7	03	
22	Y8	02	
24	Y9	01	
26	Y10	00	
06	PLN	NADEN	Enables the next address to be loaded from the microprogram buffer NAD.
05	VTN	PLAVECN	Enables the next address to be loaded from PLAVEC.
07	MPN	PLAMAPN	Enables the next address to be loaded from PLAMAP.
32	CI	5V	External incrementer for Program Counter is held high and so disabled.

Table 3.5 2910 PIN DESIGNATIONS

Table 3.6 SYSTEM MICRO-INSTRUCTION WORD - DETAILED

	2901A				2910			2932																	
	0	1-3	4-9		10-13	14	15	16-19	20	21	22	23	24-25	26-27	28-31	32-34	35-37	38-39	40	41-43	44-55			
	2901A Control Field				2910 Control Field	ROMADLDN	TMRENB	2932 Control Field		LOADSN	WRITE	SELR2	R1 Field	R2 Field	GEN Purpose Field	CR Field	D Lines Emitters Select	CPU Cycle Select Field	DER	Test Field	NAD FIELD			
* Default	/0	/1		/22	/E	/1	/1	/4	/0	/1	/0	/0	/2	/2	/0	/0	/1	/0	/0	/7	/000			
	CARIN	LDQ	0	APQ	0	JZ	0	R1A;		PRST	0	CARY 32	LDM	WR,	R2B	R1M1	0	R2M1	0	NOP	0	CRNC	0	SEL8251	0	CY225	0	DE	PAF	0	NATEST	NACALLM
		FY	1	APB	1	CJS	1	RCTLD	TMRENBN	PSUS	1			GFLD		R1P1	1	R2P1	1	GPSCEI	1	CRRTN	1	DECST	1	CY270	1		Y15	1	NAPRESOF	NASAVE
		LDRAYA	2	Q	2	JMAP	2			PSHD	2					INHR1	2	INHR2	2	GPLRLD	2	CRIO	2	DEIPL	2	CY360	2		S1G	2	NAINST	NATRAS
		LDRAYF	3	B	3	CJP	3			POPS	3					LDR1	3	LDR2	3	GPBITH	3	CRFLO	3	DEDIC	3	WAIT	3		ZERO	3	NARUN	NATRAP
		SLRAQ	4	A	4	PUSH	4			FPC	4									GPKE	4	CRLOG	4	DEALUX	4				YOXY1	4	NALA	NARPA
		SLRA	5	DPA	5	JSRP	5			JMPD	5									GPDIV	5	CRAR	5	DEPSW	5				RUNIR	5	NAPWR	NALDSP
		SRRAQ	6	DPQ	6	CJV	6			PSHP	6									GPMUL	6	CRCMP	6	DEDI	6				CVAL	6	NAPREAL	NARAD
		SRRA	7	DARITH	7	JRP	7			RTS	7									GPCHA	7	CRSLA	7	DE32	7				BID	7	NATSOC	NACOMRZO
				QMAM1	8	RFCT	8			FR	8									GPTMF	8										NATROC	NATRAPER
				BMAM1	9	RPCT	9			FPR	9									GPTMP	9										NAINT	NAERR1
				QM1	A	CRTN	A			FPLR	A									GPTME	A										NASD	NAMIOPER
				BM1	B	CJPP	B			JMPR	B									GPBOF	B										NALM2	NAUSEZO
				AM1	C	LDCT	C			JPPR	C									GPFLOT	C										NASTORE	NAUSERET
				AMDM1	D	LOOP	D			JSBR	D									GFETCH	D										NAPAF	NAWAITST
				QMDM1	E	CONT	E			JSPR	E									GPAF	E										NAFETCH	NASSTFLO
				MDM1	F	TWB	F			PLDR	F									GPVAL	F										NAFOUR	NAFPPABS
				AMQM1	10																										NAVISU	NAINHSAV
				AMBM1	11																								GPextension		NASENDAD	NAEND
				MQM1	12																										NARIPL	NAFLAG
				MBM1	13																										NAFUNCT	NAPAFRF
				MAM1	14																										NACRUNCH	NAPAFRB
				DMAM1	15																										NACRLOG	NAINH
				DMQM1	16																										NACRAR	NABUS
				DM1	17																								TMRINH	1	NADECPUP	ECLAT1
				AOQ	18																								GPRESET	2	NARM2	ECLAT2
				AOB	19																								GPEX	3	NAPACC	ECLAT3
				QLOG	1A																								GPMAD	4	NAMCL	ECLAT4
				BLOG	1B																								SELSPBUF	5	NASC	
				ALOG	1C																								GPSP	6	NAPAFTCH	
				DOA	1D																								INHIOP	7	NASTOV	
				DOQ	1E																										NADAC1	
				DLOG	1F																										NADAC3	
				AAQ	20																										NADS1	
				AAB	21																										NAWAIT	
				NUL	22																										NAWRIBH	
				DAA	25																										NAFINBH	
				DAQ	26																										NABHPAF	
				A1AQ	28																										NAPAFW2	
				D1AA	2D																										NACRZ3	
				D1AQ	2E																										NAITRT	
				AXQ	30																										NASITRT	
				AXB	31																										NACLEAR	
				DXA	35																										NASTAT	
				DXQ	36																										NALOCK	
				AXNB	39																										NABAWOFF	
				QI	3A																										NABOOT	
				BI	3B																										NAECLAT	
				AI	3C																										NARSTV24	
				DXQN	3E																										NASDV24	
				DI	3F																										NASCV24	

* Note: Default values are not mentioned in the COSYM - Listing (uProgram)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
				2901 Control Field (Bits 0-9)
0	ALUCIN	CARIN		This is a 1-bit field (bit 0) and its main use is as a carry bit for arithmetic operations in the 2901. When the 2901 is not performing arithmetic operations this bit can be used for the following purposes: - The carry bit of the Arithmetic/Logic unit in the MIOP has to be programmable for both IOP and MMU operations. During IOP operations the data length (which was loaded into the IOP register in two's complement by a WER instruction) is incremented at each Break Request so that during the last transfer the carry of the last ALU stage generates the End of Range signal to the CU. For MMU operations for Table Load instructions (TL) the address data has to be transferred in transparent mode. The CARIN field is used for these two purposes as shown below: CARIN = 0 - Increment (WER) CARIN = 1 - Do Not Increment (TL) - It is used as the selection signal for the multiplexor that selects the PLR source; as shown below: CARIN = 0 - source = 2901 CARIN = 1 - source = BIEC lines - During RIT instructions for Power Failure and Real Time Clock, CARIN = 1 is used to distinguish these RIT's from any other RIT; this avoids copying the preceeding state of these two flip-flops when resetting other interrupts.
1 - 3			I8 I7 I6	2901A Destination Control (Bits 1-3)
		LDQ	000	Load Register Q (LDQ)
		FY	001	Function to Y
		LDRAYA	010	Port A to Y, Function to Port B
		LDRAYF	011	Function to Y, Function to Port B
		SRRAQ	100	Shift Right (F/2 to Port B, Q/2 to Q)
		SRRA	101	Shift Right (F/2 to Port B)
		SLRAQ	110	Shift Left (2F to port B, 2Q to Q)
		SLRA	111	Shift Left (2F to Port B)

Note: When loading MAD 64-512 bit I7 must be low (usually LDQ) is used)

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION

Micro-Instr. Bit No. 4 - 9	Signal Name	Mnemonic (COSYM)	Code	Description
				2901A Function and Source (Bits 4-9)
			I5 - I0	
		APQ	000000	A + Q
		APB	000001	A + B
		Q	000010	Q Arithmetic
		B	000011	B Arithmetic
		A	000100	A Arithmetic
		DPA	000101	D + A
		DPQ	000110	D + Q
		DARITH	000111	D Arithmetic
		QMAM1	001000	Q - A - 1
		BMAM1	001001	B - A - 1
		QM1	001010	Q - 1
		BM1	001011	B - 1
		AM1	001100	A - 1
		AMDM1	001101	A - D - 1
		QMDM1	001110	Q - D - 1
		MDM1	001111	- D - 1
		AMQM1	010000	A - Q - 1
		AMBM1	010001	A - B - 1
		MQM1	010010	- Q - 1
		MBM1	010011	- B - 1
		MAM1	010100	- A - 1
		DMAM1	010101	D - A - 1
		DMQM1	010110	D - Q - 1
		DM1	010111	D - 1
		AOQ	011000	A or Q
		AOB	011001	A or B
		QLOG	011010	Q Logic
		* BLOG	011011	B Logic
		ALOG	011100	A Logic
		DOA	011101	D or A
		DOQ	011110	D or Q
		* DLOG	011111	D Logic
		AAQ	100000	A and Q
		AAB	100001	A and B
		NUL	100010	zero
		DAA	100101	D and A
		DAQ	100110	D and Q
		AIAQ	101000	A Inverted and Q
		DIAA	101101	D Inverted and A
		DIAQ	101110	D inverted and Q
		AXQ	110000	A exclusive or Q
		AXB	110001	A exclusive or B
		DXA	110101	D exclusive or A
		DXQ	110110	D exclusive or Q
		AXNB	111001	A exclusive or B not
		QI	111010	Q Inverted
		BI	111011	B Inverted
		AI	111100	A Inverted
		DXQN	111110	D exclusive or Q not
		DI	111111	D Inverted

* BI4 = BLOG = 011011 D = DLOG = 011111

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
				2910 control Field (Bits 10-15)
10,11, 12,13		JZ	0000	Jump to Zero
		CJS	0001	Conditional Jump to Sub-routine
		JMAP	0010	Jump Map
		CJP	0011	Conditional Jump to Pipeline
		PUSH	0100	Push (conditional), Load Counter
		JSRP(NU)	0101	Cond. Jump to Sub-routine, Reg. Counter or Pipe
		CJV	0110	Conditional Jump to Vector
		JRP(NU)	0111	Conditional Jump Reg. Counter or Pipeline
		RFCT	1000	Repeat Loop, CNTR = 0
		RPCT	1001	Repeat Pipeline, CNTR = 0
		CRTN	1010	Conditional Return
		CJPP	1011	Conditional Jump Pipeline and Pop
		LDCT	1100	Load Counter and Continue
		LOOP	1101	Test End Loop
		CONT	1110	Continue
		TWB	1111	Three Way Branch
14	ROMADLDN	R1A	0	This is a one bit field (bit 14) which is used to load the contents of the NAD field into the counter register of the 2910 while it is executing an instruction, its NOP state is 1. When used with the Conditional Jump to Vector (CJV) microcommand and the value in the Test field equals 0, the number of multiple load or shifts (n) contained in instruction register K is transferred through PLAVEC in transparent mode and loaded into RCT (vector mapping is not executed due to Test = 0 not being the correct condition, the output from PLACONST making NAD01 because ROMADLDN = RDTLDN = 0). This bit can also be used to force the instructions R1 field onto the ALU's "A"input normally the R1 field uses the "B"input)
15	TMRENB	TMRENBN	0	This bit is used to inhibit a TMR during a CPU Memory Cycle. The CPU only takes the BUS in this case. See also: signal GFETCHN. TMRENB is also used to inhibit TMR in case of generation of TMP, TME (I/O cycle, External Register cycle). (See also bits 41-43).
				2932 Control Field (Bits 16-21)
16-19		PRST	0000	reset
		PSUS	0001	Suspend (High Impedance State)
		PSHD	0010	Push D
		POPS	0011	Pop S
		FPC	0100	Fetch PC (NOP)
		JMPD	0101	Jump D
		PSHP	0110	Push PC
		RTS	0111	Return S
		FR	1000	Fetch R
		FPR (NU)	1001	Fetch PC + R
		FPLR	1010	Fetch PC to R

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
16-19 (cont'd)		JMPR	1011	Jump R
		JPPR(NU)	1100	Jump PC + R
		JSBR	1101	Jump Subroutine R
		JSPR(NU)	1110	Jump Subroutine PC + R
		PLDR	1111	Load R
				2932 Control Field (Bits 16-21) cont'd
20	PCCI	CARY32	1	Program Counter Carry Input (2932) to enable operations such as PC + Ci, D + Ci, S + Ci, etc.
21	LOADSN	LDM	0	Load MAD lines
22	WRITE WRITE	WR GFLD	1	This is a one bit field (bit 22) which, when = 1, is used for the following purposes: - To either write to memory or for any other output onto the Bus, this bit is programmed at the same time as the exchange request. - To mask interrupts and Control Panel actions during the execution of the second Jump Map of an Execute instruction. This avoids the next instruction following the Execute instruction being fetched and executed (due to the reset action of the interrupt routine and the fact that the PC is already pointing to this instruction) before the Execute instruction has been completed. - To load the V24 CU sequensor during I/O instructions. - To load the General Purpose flip-flops (RUN, ENB, PI, FE, FU etc.). It also is used in both its states as follows: - To select either the MIOP Scratch Pad or the "D" Bus as input for the SPBUF8 buffer in MIOP, as shown below: WRITE = 0 - MIOP Scratch Pad is selected WRITE = 1 (in either TL or WER) - "D" Bus is selected. - In combination with the bit GPRESET (of anothor microprogram) it is used as follows: GPRESET and WRITE = 0 - the Preset Address register is reset. GPRESET and WRITE = 1 - enable Preset Address register loading.
23	SELR2	R2B	1	This is a one bit field (bit 23) which, when = 1, is used for the following purposes: - To force the instructions R2 field onto the ALU's "B" input (normally the R2 field uses the "A" input). - To distinguish between the CW2 and CW3 control words of a WER instruction. Normally after a CW1 has been written a flag is reset to indicate one more control word to write (i.e. CW2).

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
23 (cont'd)				This procedure is also followed when extended addressing is used, but in this case after the CW2 has been written the flag is set (by means of the SELR2 bit) to indicate that the next control word is a CW3 and not a CW2. - To generate the PRADCL signal that clocks the Preset Address into the PRAD register. It is also used in both its states as follows: - To select either the MIOP Scratch Pad or the "D" Bus as input for the SPBUF16 buffer in in MIOP, as shown below: SELR2 = 0 - MIOP Scratch Pad is selected SELR2 = 1 (in either TL or WER) - "D" Bus is selected.
				R1 Control Field (Bits 24-25)
24-25		R1M1	00	R1 - 1
		R1P1	01	R1 + 1
		INHR1	10	Inhibit R1
		LDR1	11	Load R1
				R2 Control Field (Bits 26-27)
26-27		R2M1	00	R2 - 1
		R2P1	01	R2 + 1
		INHR2	10	Inhibit R2
		LDR2	11	Load R2
				General Purpose Field (Bits 28-31)
28-31	None	NOP	0000	No Operation
			0001	Not used
	GPLRLDN	GPLRLD	0010	Enables PLR to be loaded
	GPBITHDLN	GPBITH	0011	Inhibits Bus access during Bit Handling Instructions and during generation of CLEARN signal.
	GPKEN	GPKE	0100	Enables bits 0-3 and 12-15 of the K register to be loaded via the "D" bus. For ML and MS instructions 0 is put into these bits and then a CJV is executed. This enables the PLAVEC to output bits K5-8 (i.e. N - the number of multiple Load/store operations) onto the NAD8-11 lines. This number is loaded into the 2910 register/counter prior to executing ML or MS instructions.
	GPDIVN	GPDIV	0101	Generates the ALUIMX3 input and ALU carry and selects either ADD or SUB operations while shifting and calculating the quotient and remainder in DV instructions.
	GPMULN	GPMUL	0110	Generates the ALUIMX1 input and selects whether or not the multiplier is to be added at each step in calculating the result of MU instructions.

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
28-31 (cont'd)	GPCHAN	GPCHA	0111	Generally used for addressing the memory in Character mode but it can also be used for the following purposes: - To clock the ALUX register. - To force RUN = 1 during the PLAMAP of an INST, and the second PLAMAP of an EXECUTE routine to avoid a branch to the IDLE state (which would happen if RUN = 0) instead of the execution of these routines.
	GPTMFN	GPTMF	1000	Enables the TMFN signal for the FPP.
	GPTMPN	GPTMP	1001	Enables the TMPN signal for the Control Units.
	GPTMEN	GPTME	1010	Enables the TMEN signal for the External Registers.
	GPBOFN	GPBOF	1011	Enables the BOFFN signal for the FPP.
	GPFLOACTN	GPFLOACT	1100	Enables the FLOACT signal for the FPP.
	GFETCHN	GFETCH	1101	Indicates all Fetch cycles to the FPP and Preset Logic. Also restart of CPU sequensor after TMRINH.
	GPAFN	GPAF	1110	Enables PAFN to be tested instead of PAF. This is necessary when executing a CJV when PAF = 0.
	None	GPVAL	1111	Enables an extension of the GP field functions to be programmed when non of the other GP functions are needed. Note: This extension is provided by the TEST field bits (bits 41 to 43) and bit 28=1 (GPO=1).
			1xxx	All codes 1000 to 1111 will provide this extension too.
				Condition Register (CR) Field (Bits 32-34)
32-34		CRNC	000	Not Changed
		CRRTN	001	Return
		CRIO	010	Input/Output
		CRFLO	011	Floating Point
		CRLOG	100	Logic
		CRAR	101	Arithmetic
		CRCMP	110	Compare
		CRSLA	111	Shift left Arithmetic (during SLA and DV instructions)
35-37		D0 D1 D2		Select D lines Field (Bits 35-37)
	SEL8251N		000	Enables 8251 to ALU (D-Bus in inactive state: /FFFF)
	DECST	DECST	001	Enable Constant to D
	SELIPLN	DEIPL	010	Enable IPL to D
	SELDICN	DEDIC	011	D00-07 = 0; D08-15 = NAD4-11
	SELALUN	DEALUX	100	Enable ALUX to D
	SELPSW	DEPSW	101	Enable PSW to D
	SELDIN	DEDI	110	Enable DI bits 00-15 to D
	SELADN	DE32	111	Enable 2932 to D
	Note: D0=1 enables 2901 to D0 of 2907/2917			

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
				Sequensor Control Field (Bits 38-39)
38-39		CY225	00	CPU Cycle 225 nS
		CY270	01	CPU Cycle 270 nS
		CY360	10	CPU Cycle 360 nS
		WAIT	11	CPU Cycle WAIT
				Data Exchange Request (Bit 40)
40	DE	DE	1	Active to initiate a Bus Cycle if no T3 type of instruction was fetched.
				Test Field (Bits 41-43 enabled with bit 28=0)
41-43	PAFTEST	PAF	000	Page Fault during MMU operations
	ALU15	Y15	001	Least significant ALU bit (ALU15)
	ALUSIGNE	SIG	010	Sign bit of ALU (ALUSIGNE)
	ALUZERO			(ALUZERO)
	ALUØX1	YOXY1	100	XOR between the 2 most significant ALU bits
	IRUNA	RUNIR	101	Test for Run and Interrupt
	CONDVAL	CVAL	110	Condition Valid (for Conditional Jumps)
	BID	BID	111	=5V (NOP) (Unconditional test input). Note: When GPO=1 the Test Field Bits are considered as an extension to the GP Field and testing is impossible.
				GP Extension Field (Bits 41-43 enabled with Bit 28=1)
	TMRENB	TMRINH	001	Inhibit TMR (used in old versions only, see bit 15)
	GPRESETN	GPRESET	010	Reset SOPA Function (MIOP)
	GPEXN	GPEX	011	Enables Translation Mode during EL and ES instruction.
	GPMADN	GPMAD	100	Load MAD buffer bits 64, 128, 256 and 512 if ALUTI1, 2 are zero.
	SELSPBUFN	SELSPBUF	101	MIOP Enable Scratch pad buffer on D-bus.
	GPSPN	GPSP	110	(MIOP) Enable Flag for CW3 (IOP). Enable Scratch Pad + Buffer Clock SPBUFCL.
	ENBIOP	INHIOP	111	To block IOP in case of CPU action in scratch Pad MIOP. This command is active if GPO=1 and TESTO = 1 (bits 28 and 41) and is also active when GPMAD, SELSPBUF and GPSP are active.
				Next Address Field (Bits 44-55)
				This is a twelve bit field (bits 44 to 55) whose main function is to define the address of the next instruction. When the next instruction is sequential, this field can be used for other purposes described on the next page.

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
41-43 (cont'd)				- The NAD03 bit is used in combination with SEL8251 to select the 8251 chip of the HHP serial device. - The NAD06 bit is used in combination with SEL8251 to select the 8251 chip of the V24 serial device on the P857E. - The NAD05 bit is used in combination with SEL8251 to inhibit the 2901 outputs while reading one of the 8251 devices connected to the ALU Bus (NAD08 being used to define the direction of data flow on the ALU Bus). At the same time NAD08 is used as the RDN input, NAD09 is used as the WRN input, and NAD10 as the C/DN input to the 8251 devices.
44-55		NATEST	011011111111	/6FF
		NAPRESOF	010101000000	/540
		NAINST	010101100111	/567
		NARUN	010101010000	/550
		NALA	010111010000	/5D0
		NAPWR	010101000101	/545
		NAPREAL	010111011001	/5D9
		NATSOC	011011010000	/6D0
		NATROC	010110101101	/5AD
		NAINT	011001000000	/640
		NASD	010100001110	/50E
		NALM2	000001010101	/055
		NASTORE	010000111001	/439
		NAPAF	000001110010	/072
		NAFETCH	000000010010	/012
		NAFOUR	010111101100	/5EC
		NAVISU	011000000010	/602
		NASENDAD	011001100110	/666
		NARIPL	011000100000	/620
		NAFUNCT	000000100000	/020
		NACRUNCH	000010110000	/0B0
		NACRLOG	000110011000	/198
		NACRAR	010010110001	/4B1
		NADECPUP	010100110000	/530
		NARM2	000001010111	/057
		NAPACC	010110001000	/588
		NAMCL	010100110111	/537
		NASC	010100011000	/518
		NAPAFTCH	000001110000	/070
		NASTOV	000110001110	/18E
		NADAC1	001000110010	/232
		NADAC3	001000101011	/22B
		NADS1	000110110111	/1B7
		NAWAIT	011011100000	/6E0
		NAWRIBH	000111100111	/1E7
		NAFINBH	000111101000	/1E8
		NABHPAF	000101000011	/143
		NAPAFW2	000001101010	/06A
		NACRZ3	000100010110	/116

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

Micro-Instr. Bit No.	Signal Name	Mnemonic (COSYM)	Code	Description
44-45 (cont'd)		NAITRT	011001000000	/640
		NASITRT	001000010010	/212
		NACLEAR	011001111000	/678
		NASTAT	010111000011	/5C3
		NALOCK	010111110100	/5F4
		NABAWOFF	000100100000	/120
		NABOOT	010110000100	/584
		NAECLAT	000000010011	/013
		NARSTV24	010110100011	/5A3
		NASDV24	011000000101	/605
		NASCV24	001101001001	/349
		NACALLM	010100000011	/503
		NASAVE	010110111000	/5B8
		NATRAS	000001100011	/063
		NATRAP	010011111111	/4FF
		NARPA	010110001111	/58F
		NALDSP	010110001100	/58C
		NARAD	001010100000	/2A0
		NACOMRZ0	011101010110	/756
		NATRAPER	011101010011	/753
		NAERR1	011100110001	/731
		NAMIOPER	011101100101	/765
		NAUSEZ0	011010010000	/690
		NAUSERET	011010010101	/695
		NAWAITST	000001100111	/067
		NASSTFL0	011000101011	/62B
		NAFPPABS	011010100000	/6A0
		NAINHSAV	011010100101	/6A5
		NAEND	011101001101	/74D
		NAFLAG	001110100111	/3A7
		NAPAFRF	000011100110	/0E6
		NAPAFRB	000011110011	/0F3
		NAINH	011010100110	/6A6
		NABUS	011110100100	/7A4
		ECLAT1	000110001000	/188
		ECLAT2	101100110100	/B34
		ECLAT3	111100000001	/F01
		ECLAT4	10001111	/8F

Table 3.7 SYSTEM MICRO-INSTRUCTION WORD - DETAILED DESCRIPTION (CONT'D)

3.5.3 NEXT ADDRESS GENERATORS

There are 3 Next Address (NAD) Generators which enable a 12-bit code to be written onto the NAD lines; the 3 generators are: PLAMAP, PLAVEC and the NAD Field of the Micro-inst being executed.

PLAMAP (Table 3.8)
PLAMAP is a Programmable Logic Array which senses the machine states at its inputs. When enabled, (PLAMAP = 0) by the execution of the 2910 Micro-inst JMAP a code appears at the output and is written on the NAD lines. Note that PLAMAP only generates 8 bits (NAD 02-09) and bits 00, 01 and 10 are held at "0" and bit 11 is held at "1".

The inputs to PLAMAP which indicate the machine states are:

- PUPFE - Control Panel interrupt
- RUNIRN - RUN-not or interrupt or Control Panel function.
- FUN - Flag User/System mode
- D15 - Bit 15 of instruction word
- 15R2N - Reg A15 is given in the R2 field
- OR2 - Zero in R2 field
- D10 - Bit 10 of the instruction word
- D09 - Bit 9 of the instruction word
- D08 - Bit 8 of the instruction word
- 15R1N - Reg A15 is given in the R1 field
- OR3 - Zero in R3 field (T8 instructions)
- D04 - Bit 4 of the instruction word
- D03 - Bit 3 of the instruction word
- D02 - Bit 2 of the instruction word
- D01 - Bit 1 of the instruction word
- D00 - Bit 0 of the instruction word

	INPUTS															OUTPUTS												FUNCTION
	D 0	D 0	D 0	D 0	D 0	0 R 3	1 R 1 N	D 5	D 8	D 9	0 R 2	1 R 2 N	D 5	F 1	R U N	P U P		NAD LINES R E	0	1	2	3	4	5	6	7	8	9	10	11	
																			0	0	H	H	H	H	H	H	H	H	0	1	
00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	L			A	A	A	.	.	.	A	A					Interrupt or Idle
01	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	H			A	A	A	A	.	.	A	A					Panel
02	L	H	-	-	-	-	-	-	-	-	-	-	-	-	L	L			A	.	.	.	.	.	.	.					T8 K01
03	L	-	H	-	-	-	-	-	-	-	-	-	-	-	L	L			.	A	.	.	.	.	.	.					T8 K02
04	L	-	-	H	-	-	-	-	-	-	-	-	-	-	L	L			.	.	A	.	.	.	.	.					T8 K03
05	L	-	-	-	H	-	-	-	-	-	-	-	-	-	L	L			.	.	.	A	.	.	.	.					T8 K04
06	L	-	-	-	-	H	-	-	-	-	-	-	-	-	L	L			.	.	.	.	.	.	.	A					T8 OR3
07	H	H	-	-	-	-	-	L	L	-	-	-	-	-	L	L			A	.	.	.	.	A	.	.					T1 K01
08	H	-	H	-	-	-	-	L	L	-	-	-	-	-	L	L			.	A	.	.	.	A	.	.					T1 K02
09	H	-	-	H	-	-	-	L	L	-	-	-	-	-	L	L			.	.	A	.	.	A	.	.					T1 K03
10	H	-	-	-	H	-	-	L	L	-	-	-	-	-	L	L			.	.	.	A	.	A	.	.					T1 K04
11	H	-	-	-	-	H	-	L	L	L	-	-	-	-	L	L			.	.	.	.	.	.	.	A					T1 OR1
12	H	-	-	-	-	-	-	-	L	L	-	-	H	-	L	L			.	.	.	.	.	.	A	.					T1 K15
13	H	-	-	-	-	-	-	-	L	L	H	-	-	-	L	L			.	.	.	.	A	.	.	.					T1 OR2
14	H	L	L	L	L	-	-	-	L	L	-	-	-	-	L	L			.	.	.	.	.	A	A	.					LDR
15	H	L	L	L	H	-	-	-	L	L	-	-	-	-	L	L			.	.	.	.	.	.	A	A					ABR
16	H	L	H	H	H	-	-	-	L	L	-	-	-	-	L	L			A	.	.	.	A	A	A	A					TRAP T1 OPC7
17	H	-	-	-	-	-	L	-	-	-	-	-	-	-	L	L	L		A	A	A	A	A	A	A	A					TRAP T1 to T7 for FU.15R1
18	H	-	-	-	-	-	-	-	L	H	H	-	-	-	L	L			.	.	.	A	A	.	A	.					T2
19	H	-	-	-	-	-	-	-	L	H	L	-	-	-	L	L			A	.	.	.	A	.	.	.					T3
20	H	-	-	-	-	-	-	-	H	-	H	-	-	-	L	L			.	.	.	.	.	.	A	.					T4 and T6
21	H	-	-	-	-	-	-	-	H	L	-	-	-	-	L	L			.	.	A	.	A	.	.	.					T4 and T5
22	H	-	-	-	-	-	-	-	H	H	-	-	-	-	L	L			.	A	.	.	A	.	.	.					T6 and T7
23	H	L	L	L	L	-	-	-	L	H	-	L	-	-	L	L			.	A	.	.	.	.	.	.					T3B LDR STR
24	H	L	H	H	H	L	-	-	L	H	-	L	-	-	L	L			.	A	A	.	.	.	.	.					T3B MLR MSR
25	H	L	H	H	H	-	-	H	L	H	-	L	-	-	L	L			.	A	A	.	.	.	.	.					T3B MLR MSR
26	H	H	H	H	L	H	-	L	L	H	L	L	L	-	L	L			.	A	A	A	.	.	A	.					T3B RTN A15
27	H	-	-	-	-	-	-	-	L	H	-	L	-	L	L	L			.	.	.	.	.	A	A	A					T3B.FU

Table 3.8 PLAMAPA

	INPUTS															OUTPUTS												FUNCTION
	D0	D0	D0	D0	D0	01R	15R	D0	D0	D0	01R	15R	DFN	FUN	RUN	PUF	NAD LINES												
	01	02	03	04	3	1N	8	09	02	2N	5	N		IRN			0	1	2	3	4	5	6	7	8	9	10	11	
																	00		H	H	H	H	H	H	H	H	0	1	
28	H	-	-	-	-	-	-	-	L	H	-	L	H	-	L	L			.	.	.	.	.	.	A	.			T3B.K15
29	H	L	L	L	L	H	-	L	L	H	-	L	-	-	L	L			.	.	.	A	.	.	.	.			T3B.OR1.OPC0
30	L	L	H	L	L	H	-	-	-	-	-	-	-	-	L	L			A	A	A	A	A	A	A	A			TRAP T8 FU HLT, INH, RIT
31	L	L	H	H	H	-	-	H	L	-	-	L	-	L	L	L			A	A	A	A	A	A	A	A			TRAP T8 FU SH NORM 15R2
32	L	H	L	L	-	L	-	-	-	-	-	-	-	-	L	L			A	A	A	A	A	A	A	A			TRAP T8 FU I/O INSTR
33	L	H	L	H	-	-	-	-	-	-	-	-	-	H	-	L			A	A	A	A	A	A	A	A			Trap T8 K15 RF or RB
34	L	H	H	H	-	L	-	-	-	-	-	-	-	L	L	L			A	A	A	A	A	A	A	A			Trap T8 FU RER or WER
35	L	H	H	H	-	H	-	-	-	-	-	L	-	L	L	L			A	A	A	A	A	A	A	A			Trap T8 FU Move 15R2
36	H	L	H	H	H	H	-	L	-	-	-	-	-	L	L	L			A	A	A	A	A	A	A	A			Trap FU TL, TS
37	H	H	L	H	L	L	-	-	-	-	-	-	-	L	L	L			A	A	A	A	A	A	A	A			Trap FU EL, ES
38	H	H	L	H	L	-	-	H	-	-	-	-	-	L	L	L			A	A	A	A	A	A	A	A			Trap FU EL, ES
39	L	L	H	H	H	-	-	-	-	H	-	-	-	-	L	L			.	.	.	.	.	.	A	.			Shifts
40	L	L	H	H	H	-	-	-	H	-	-	-	-	-	L	L			.	.	.	.	.	A	.	.			Shifts
41	L	L	H	H	H	-	-	H	-	-	-	-	-	-	L	L			.	.	.	.	A	.	.	.			Shifts
42	H	H	L	-	-	H	-	L	H	-	-	-	H	-	L	L			.	.	.	A	.	.	.	.			Bit handling
43	H	L	L	L	L	-	-	-	-	-	-	-	H	-	L	L			.	.	.	.	.	.	.	A			STORE
44	H	L	H	L	-	H	-	L	L	L	-	-	-	-	L	L			A	A	A	A	A	A	A	A			Trap T1.OR1 OPC4 and OPC5
45	H	H	H	L	-	-	-	-	-	-	-	-	-	-	L	L			.	.	.	.	.	.	.	A			CHARACTER INSTR.
46	H	H	L	-	-	H	-	L	L	L	-	-	H	-	L	L			A	A	A	A	A	A	A	A			Trap T1.OR1.K15 OPC8 to 11
47	L	L	L	L	L	L	-	-	-	-	-	-	-	-	L	L			.	.	.	.	.	.	A	.			LDK OR1N

Table 3.8 PLAMAPA (CONT'D)

	K LINES				NAD LINES									FUNCTION
	0 - 3	4 - 7	8 - 11	12 - 15	4							11		
					H	H	H	H	H	H	H	H	48	
STX														
00	L	L	H	H	.	.	.	A	.	.	.	.		Shift count
01	L	L	H	H	.	.	.	.	A	.	.	.		Shift count
02	L	L	H	H	.	.	.	.	.	A	.	.		Shift count
03	L	L	H	H	.	.	.	.	.	.	A	.		Shift count
04	L	L	H	H	.	.	.	.	.	.	.	A		Shift count
05	H	H	-	-	A	.	.	.	.	.	.	.		T2 to T7 K01
06	H	-	H	-	.	A	.	.	.	.	.	.		K02
07	H	-	-	H	.	.	A	.	.	.	.	.		K03
08	H	-	-	H	.	.	.	A	.	.	.	.		K04
09	H	-	-	-	.	.	.	.	.	A	.	.		R1=0
10	H	-	-	-	.	.	.	.	A	.	.	.		K15
11	H	L	H	-	A	A	A	A	A	A	A	A		Trap T2
12	H	H	L	-	A	A	A	A	A	A	A	A		Trap T2
13	H	H	L	-	A	A	A	A	A	A	A	A		Trap T2
14	H	H	L	-	A	A	A	A	A	A	A	A		Trap T2
15	H	H	L	-	A	A	A	A	A	A	A	A		Trap T2
16	H	H	H	H	A	A	A	A	A	A	A	A		Trap T2
17	H	L	-	-	A	A	A	A	A	A	A	A		Trap T2
18	H	H	L	-	A	A	A	A	A	A	A	A		Trap T2
19	H	H	H	L	A	A	A	A	A	A	A	A		Trap T2
20	H	H	H	H	A	A	A	A	A	A	A	A		Trap T2
21	H	H	H	H	A	A	A	A	A	A	A	A		Trap T4 to T7
22	L	H	H	L	.	.	.	.	.	.	.	A		String handling
23	L	H	H	L	.	.	.	.	.	A	.	.		MVS
24	L	H	H	L	.	.	.	.	A	.	.	.		MVA
25	L	H	H	L	.	.	.	.	A	A	.	.		CS
26	L	H	H	L	.	.	.	A	.	.	.	.		CA
27	L	H	H	L	A	.	.	.	.	.	.	.		Extension PEAB
28	L	H	H	L	.	.	.	.	.	A	.	.		R3 FREE
29	L	H	H	L	.	.	.	.	A	.	.	.		
30	L	H	H	L	.	.	.	A	.	.	.	.		
31	L	H	H	L	.	.	A	.	.	.	.	.		OPC' from E0 to FE
32	L	H	H	L	.	A	.	.	.	.	.	.		
33	H	L	H	H	.	.	.	.	.	.	.	A		Increment P for MLK
34	H	H	L	H	.	.	.	.	.	.	.	A		Increment P for DAK
35	H	H	L	H	.	.	.	.	.	.	.	A		Increment P for DSK
36	L	L	L	L	.	.	.	.	A	.	.	.		Register number for ML.MS
37	L	L	L	L	.	.	.	.	.	A	.	.		Second PLAVEC valid after resetting of the Bits K00 to K03 and K12 to K15
38	L	L	L	L	.	.	.	.	.	.	.	A		
39	L	L	L	L	.	.	.	.	.	.	.	A		
40	H	L	L	L	.	.	.	.	.	A	.	.		AB
41	H	L	H	L	A	A	A	A	A	A	A	A		Trap OPC5.OR1
42	H	L	H	H	A	A	A	A	A	A	A	A		Trap OPC6.OR1
43	H	L	L	L	A	A	A	A	A	A	A	A		Trap OPC1.K15
44	H	H	L	H	A	A	A	A	A	A	A	A		Trap OPC8.K15
45	H	H	H	L	.	.	.	.	A	.	.	A		LCK
46	H	H	H	L	.	.	.	.	.	.	.	A		CCK, CWK
47	L	H	H	L	.	.	A	.	.	.	.	A		TRAP PEAB /F4

Table 3.9 PLAVECA

Test Bits 0 1 2	Signal Input	Description
0 0 0	PAFTEST	Page Fault
0 0 1	ALU15	The least significant ALU bit.
0 1 0	ALUSIGNE	The most significant bit of the ALU output.
0 1 1	ALUZERO	Indicates that the result of an ALU operation is zero.
1 0 0	ALUOX1	Shift normalise, an exclusive OR between bits 0 and 1.
1 0 1	IRUNA	Test for Run and Interrupt.
1 1 0	CONDVAL	Branch instruction, condition valid (see Table 3.11).
1 1 1	BID	Conditional Branch Test, gives facility for conditional branching during the microroutine. BID is held at logic 1 so the result of the test is always known (condition true)

Table 3.10 TEST INTERNAL RESULT

KO5	KO6	KO7	CRO	CR1	CONDVAL
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

Table 3.11 BRANCH INSTRUCTION - CONDITION VALID

PLAVEC (Table 3.9)

The PLAVEC is a Programmable Logic Array which receives the contents of the K Register (instruction format) as its input. When enabled (PLAVECN = 0) by the execution of the 2910 Micro-inst CJV a code appears at the output and is written onto the NAD lines. Note that PLAVEC only generates 8 bits (NAD 04-11) and bits 00, 02, 03 are held at "0" bit 01 is dependant on the ROMADLDN signal. With ROMADLDN active the NAD lines will always have the value /0XX and when not active the value /4XX.

NAD FIELD (Explicit Addressing)

The NAD field is Micro-Program bits 44-55 of the Micro-inst being executed. When enabled (NADEN = 0) the content of the NAD field is written onto the NAD lines in true value. (Note that the NAD field is also used to write a constant onto the NAD lines and then onto Bus D (SELCONSTN = 0)).

3.5.4 TEST EXTERNAL RESULT (TABLE 3.10)

During certain routines the 2910 tests signal TESTN to find a result. Signal TESTN has the following significance:

. TESTN = 1 Test failed
. TESTN = 0 Test passed

Signal TESTN is generated by a multiplexer 74S151 and the tests carried out are indicated in Table 3.10, note that the Test Bits 0, 1 and 2 are from the Test Field of the Micro-inst being executed. One of the inputs CONDVAL (Condition Valid) is for Branch Instructions, see Table 3.10 and 3.11.

3.6 SPECIFYING THE CPU CYCLE LENGTH (FIGURE 3.6)

There are 4 CPU cycles, 3 of fixed length - 225 nS, 270 nS, 360 nS and one cycle of not-fixed length is called WAIT. The type of cycle (fixed length or WAIT) is specified by the SEQ Field of the micro-instruction currently being addressed. The WAIT cycle is always specified when the CPU Sequensor must wait for an external event to take place. The selection of the WAIT cycle is made at system design time and is then programmed in the SEQ Field of the microinstruction PROM. The CPU cycle length is long enough to execute an operation and address and access the Microprogram for the next address.

3.6.1 LOAD MADS OPERATIONS (FIGURE 3.6A)

In this type of operation before MADS can be loaded by the 2932 the value must be prepared by the 2901. As can be seen in Figure 3.6A the 2910 has already prepared the ROMAD lines and so the cycle length is determined by the operating times of the 2901 and 2932.

3.6.2 CONDITIONAL JUMP OPERATIONS (FIGURE 3.6B)

In this operation the 2910 cannot prepare the ROMAD lines until the result of a test is known. This test is carried out by the 2901 and depending on the result the 2910 gives the next micro-program address. At the end of the 2910 operation a PROM access time of 50 to 70 nS must be allowed.

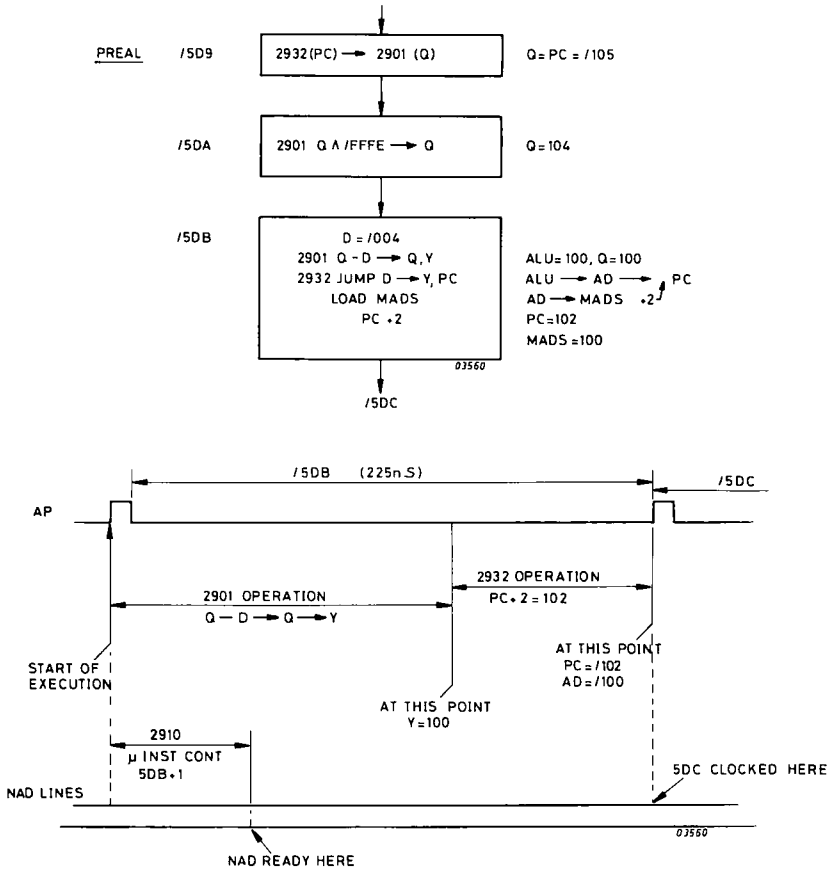


Figure 3.6A OPERATION LOAD MADS

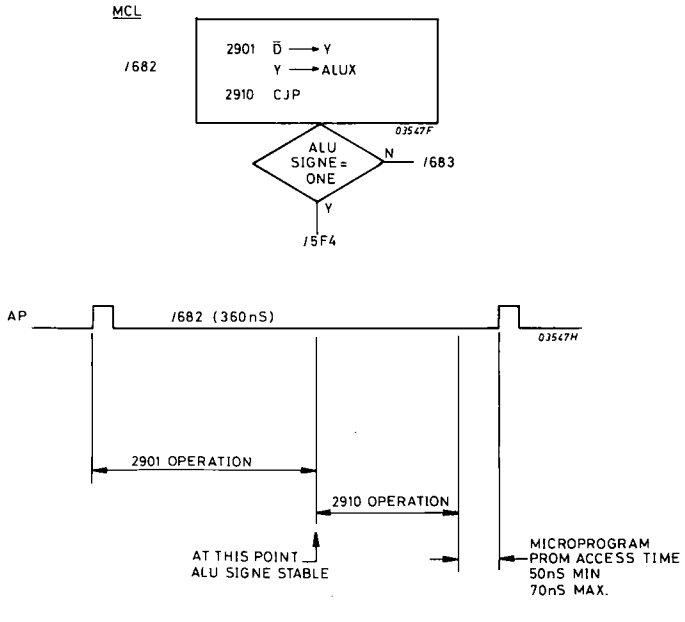


Figure 3.6B CONDITIONAL JUMP OPERATION

3.7 POWER-ON AND ENABLE CLEARN (FIGURE 3.7)

At Power-on time, signals RSLN and CLEARN are generated to ensure an orderly start procedure. RSLN is from the Power Supply and CLEARN from the CPU (C7E2/A). Both signals form a part of the GP Bus and are available to all system units connected to the Bus.

3.7.1 RESET CONTROL PANEL INTERFACE (C7E2/A)

Signal RSLF is high to reset the Control Panel Interface Device (8251A) causing it to go into Idle Mode. The 8251A stays in Idle Mode until the Mode Instruction is executed.

3.7.2 RESET MICROPROGRAM REGISTER (CP7R/C)

Signal RSLAN resets the Microprogram Register causing signals ROMADI 0, 1, 2, 3 to be reset (value /00). Value /00 is a Jump to Zero micro-instruction at the 2910 loading the address /000 onto the ROMAD Lines which initiates the RSL Microroutine. This is the only time that Jump to Zero is used.

3.7.3 EXECUTE MODE INSTRUCTION

During the RSL Microroutine the Mode Instruction is loaded onto the ALU lines 08-15 and written into the 8251A in the following format.

ALU	08	09	10	11	12	13	14	15
	1	1	0	0	1	1	1	0
	2 Stop Bits		Parity Not Selected		8-bit character		16x Baud Rate	

3.7.4 EXECUTE COMMAND INSTRUCTION

Following the RSL Microroutine the Microprogram jumps to the MCL routine to execute the Command Instruction and enable Bus signal CLEARN. The Command Instruction is loaded onto the ALU lines 08-15 and written to the 8251A in the following format. CLEARN is generated via DTR = 0.

ALU	08	09	10	11	12	13	14	15
	0	0	0	0	0	1	0	1
	Not significant						DTR	
					Enable Receive Mode		Enable Transmit Mode	

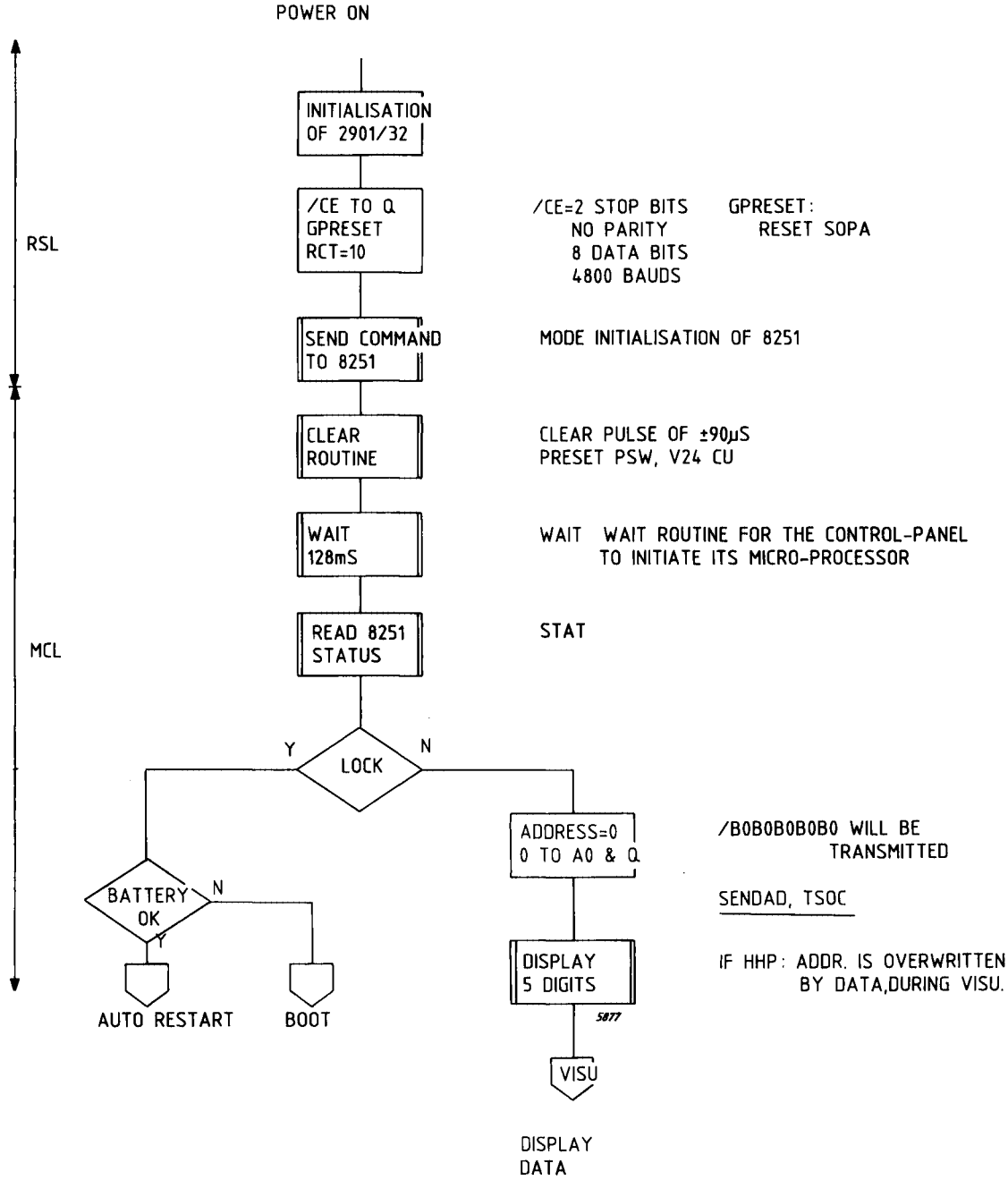


Figure 3.7A SWITCH-ON PROCEDURE

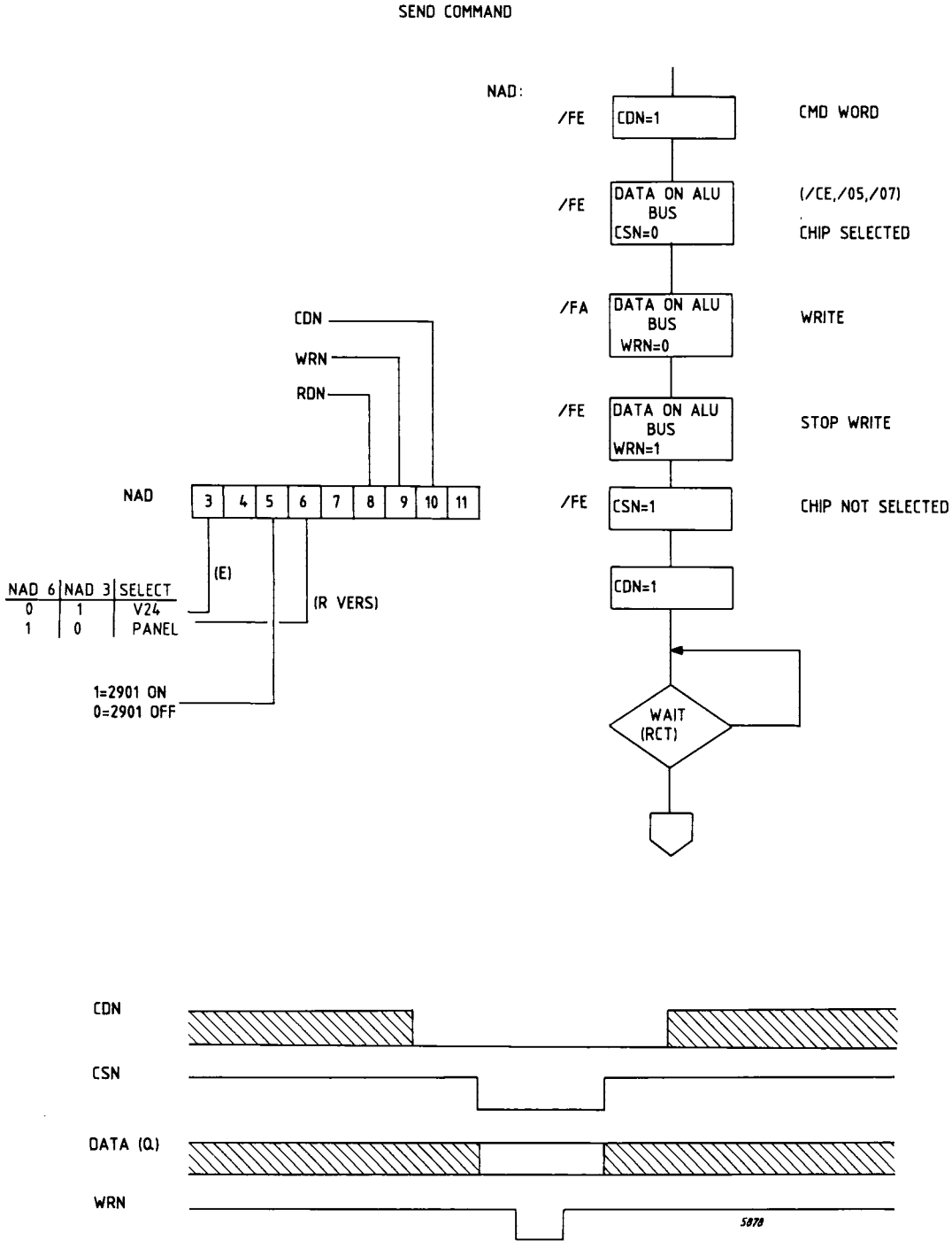


Figure 3.7B SEND COMMAND ROUTINE

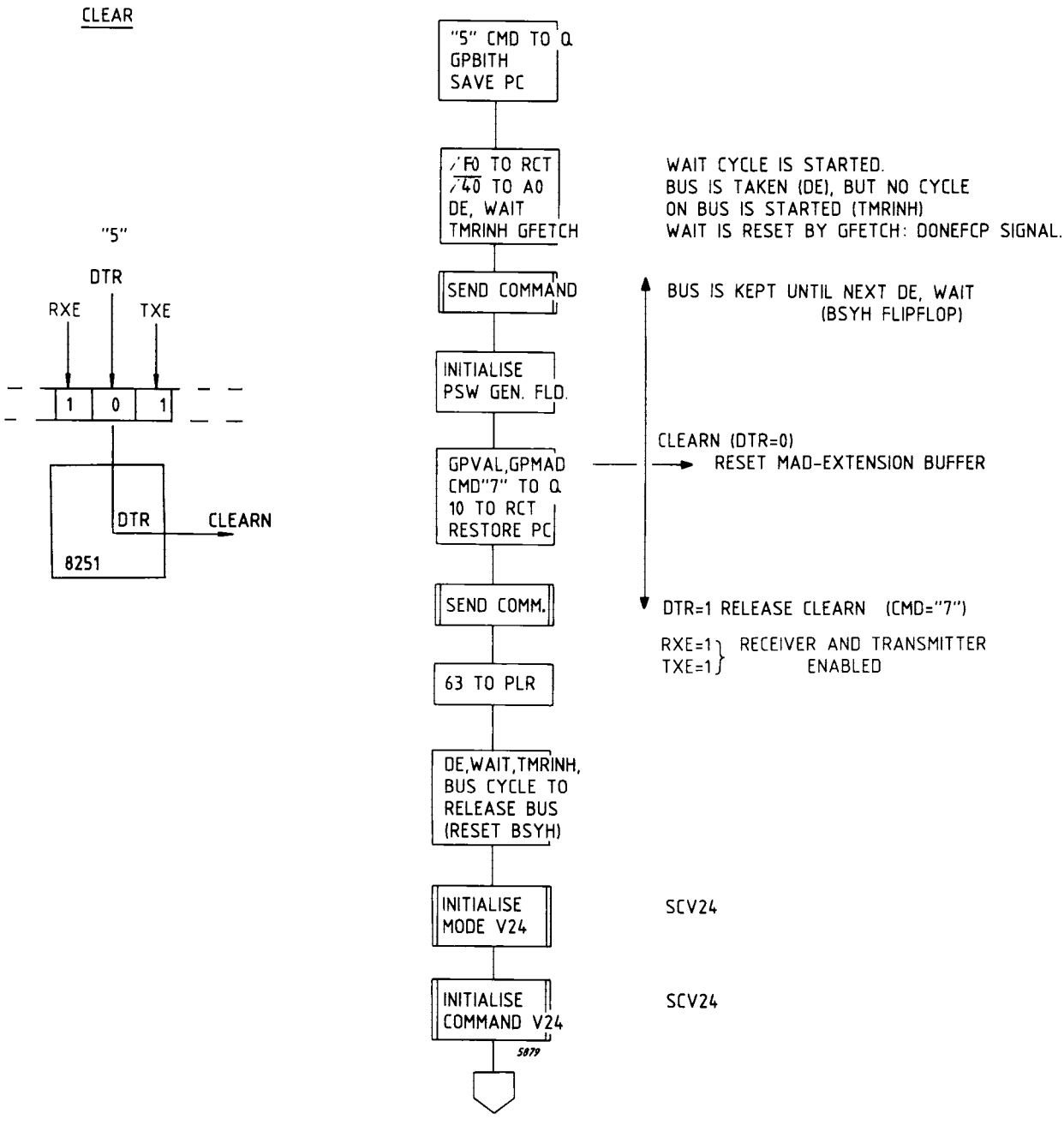


Figure 3.7C GENERATION OF SIGNAL CLEARN

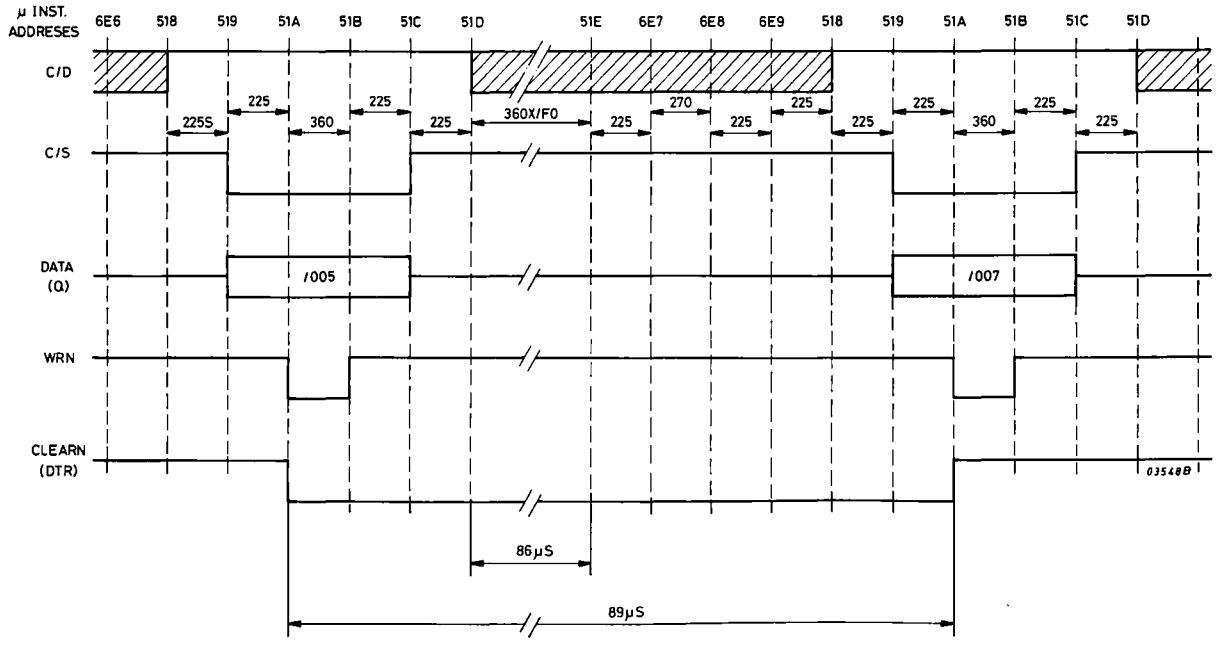


Figure 3.7D GENERATION OF SIGNAL CLEARN

3.8 CPU SEQUENSOR (FIGURE 3.8)

The CPU Sequensor is device type 74S374 containing 8 D-type latches and edge triggered F/Fs connected to count up to a maximum of 8. The Sequensor is clocked by signal OSCA on the positive going edge every 45nS, (diagram CP7R/A).

3.8.1 INITIALIZE SEQUENSOR

The Sequensor is inhibited (APD is low) until power-on time when signal RSLN goes high and START is set by RSLFN. START is selected by the Cycle Selector and will give the signal SEQIN high. SEQIN gives APD high. At the next OSCA, APD enables signal AP which indicates the start of the CPU cycle.

3.8.2 SET CYCLE LENGTH

The cycle length is specified by the micro-instruction (SEQ field) at the beginning of the cycle. The SEQ field (2 bits) programs Cycle Selector (type 74S153). The significance of the SEQ field bits is shown in table 3.7 (bits 38, 39).

3.8.3 INHIBIT AP

At the start of the CPU cycle, indicated by the rising edge of AP, APD remains high until C45N resets the signal SEQAP and START to remove APD. At the next OSCA, APD low resets the AP pulse after 90 nS.

3.8.4 CYCLE WAIT (FIGURE 3.8A)

When a Wait cycle is specified by the SEQ field the Sequensor stops counting at a count of 4 and C180 remains active high. The 5th count (C225) is inhibited by WAITSEQ (set by the SEQ field). Signal WAIT180 remains active high at the Sequensor input so that at every OSCA pulse C180 remains high.

Cycle Selector
At the end of the transfer or a timeout signal SEQWAIT is active high (see Note) at the Cycle Selector to enable SYND. The next OSC clocks and sets the WAIT F/F activating 2 signals:

- WAITN which disables WAIT180 so that C180 goes low at the next OSCA.
- WAIT which is an input to the Cycle Selector.

Signal WAIT is recognised by the select inputs (SEQ field) enabling SEQIN. Signal SEQIN enables APD. At the next OSCA AP goes high to indicate the start of the next cycle.

Note: SEQWAIT goes high on the following conditions (C7E2/F).

- TSMENDN : Trailing edge of TSMN (WRITE cycle).
- DONEFCPN : End of transfer FPP or GFETCH command (C7E1/E).
- PAFSIOPN : Page Fault or INHibit IOP and IOP not active.

WAIT is set during a SLAVE to MASTER cycle on the leading edge of TSMN via signal TSMREADN (figure 3.8B). During TSMN low, the MAD lines are maintained by means of the double buffer.

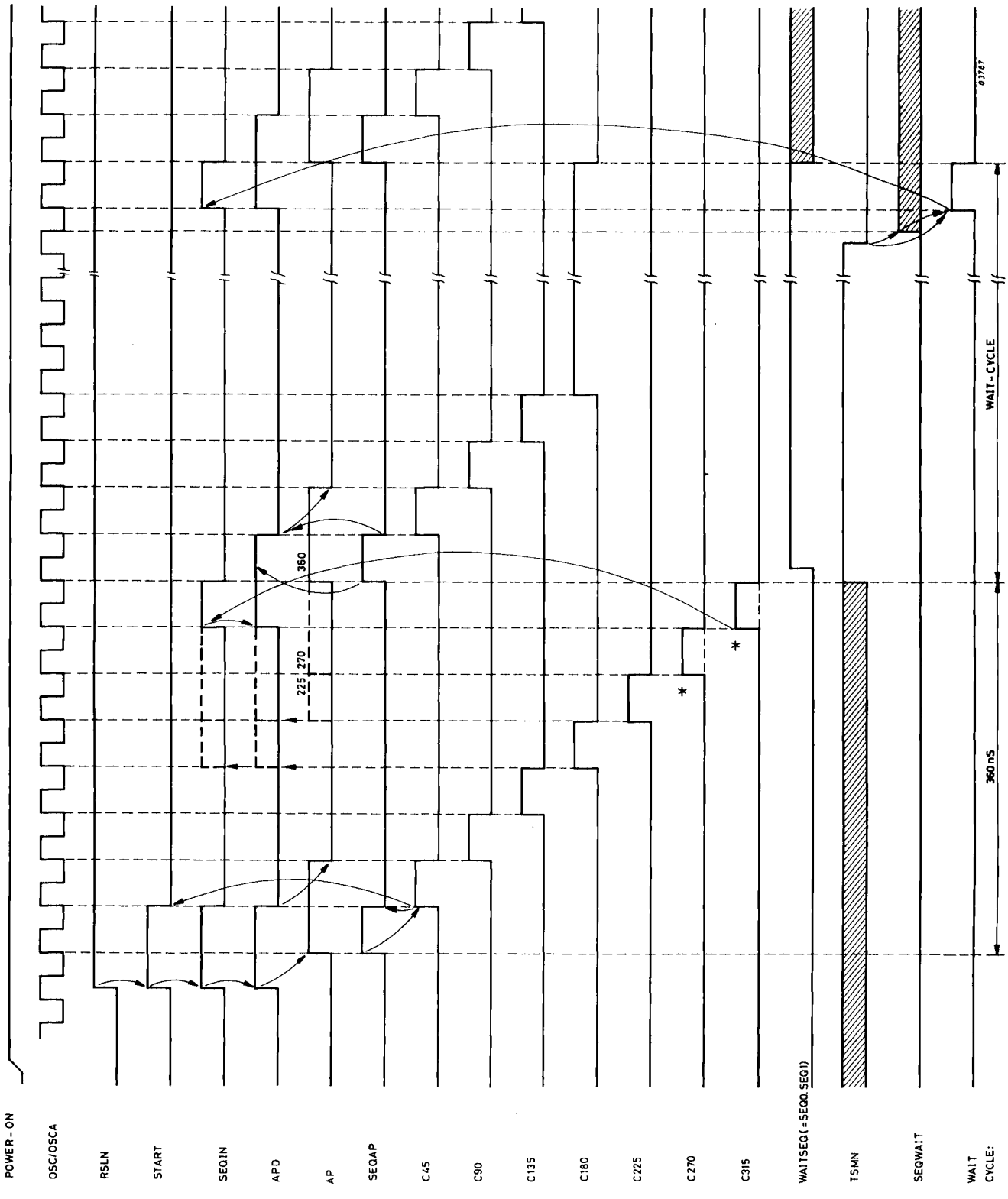


Figure 3.8A CPU CLOCK AND SEQUENSOR

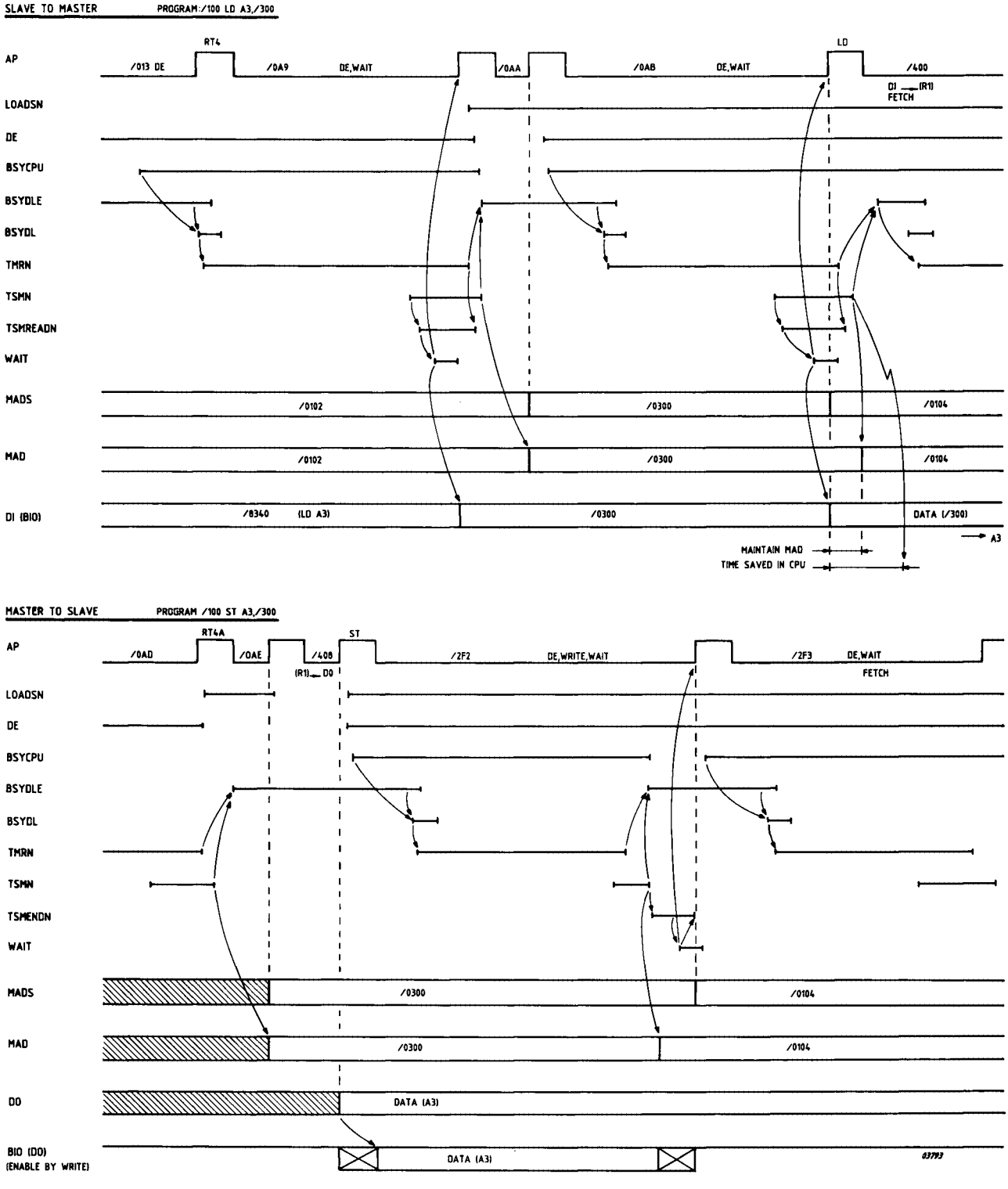


Figure 3.8B MEMORY EXCHANGES READ AND WRITE

3.8.5 CYCLES CY225, CY270, CY360

The Sequensor has 3 fixed length cycles:

- CY225, count of 5 indicated by signal C180
- CY270, count of 6 indicated by signal C225
- CY360, count of 8 indicated by signal C315.

The Cycle Selectors are already programmed at AP time so that when one of the corresponding signals is active (C180, C225, C315) then signal APD indicates end of cycle. The next OSCA pulse clocks AP and starts the next cycle.

3.9 INTERRUPTS (FIGURE 3.9)

The Interrupt Logic is implemented on card C7E2 with the exception of the encoding logic for interrupt levels 8-15 (C7E1) and 16-31 (MIOP). There are 2 types of interrupt, serial coded and parallel code; the serial coded are via Bus signal BCI and the parallel coded are via 32 interrupt lines. Before the CPU validates an interrupt (signal IR) the following sequence of events take place:

- receive serial interrupt
- encode parallel and serial interrupts
- compare the parallel with the serial encodes
- select the highest level.
- compare new level with current level (PLR).
- Update PLR

3.9.1 RECEIVING SERIAL INTERRUPT (FIGURE 3.9B)

The serial Interrupts principles of operation are already described in Chapter II. The principal components of the Serial Interrupt Logic are:

- Counter - divided by 2, this counter generates the interrupt system clock (INCL) to synchronize the C.U.s with CPU operation.
- SCT Counter - counts to 6 to clock the Source Code from the Register into the Buffer; counts to 15 to indicate the end of a "code count".
- Source Code Register - receives the 6-bit Source Code and Start Bit
- Source Code Buffer - receives the 6-bit Source code to generate on the SCINTF lines.

For purpose of this description the serial interrupt operation is described as follows:

- start exchanging interrupt code
- source code arrives
- destination and M bits arrive

START EXCHANGING INTERRUPT CODE

After Master Clear (CLEARAN) signal SCTLD is zero. As long as BCIREC stays zero (BCI=1), SCTLDEN is zero and SCTLD stays also zero. On each clockpulse (INCLAN) the SCT-counter is parallel loaded with the value 0001 and the counter output signals remain inactive (SCTCAN=1; SCINTLE=0). The clock INCLAN is inverted, and transmitted to the Interrupt Handler Chips on the Control Units, via BUS line INCL, to synchronize BCI of all Control Units.

SOURCE CODE ARRIVES

Control units which have an Interrupt Handler Chip, are able to sent a serial interrupt code consisting of a Start bit, 6 Source code bits, 6 Destination code bits and 2 spare bits.
The start bit is always zero and when it arrives via the BCI line, SCTLDEN becomes a high level. SCTLD and SCTLDDL also become a one, clocked by INCLAN.
From now on the SCT counter is stepped on each leading edge of INCLA.
The shift register SCINT is shifted on each trailing edge of INCL".

When the 6 source code bits have been shifted in, the counter will reach position 8 and SCINTLE becomes one clocking the SCINTF buffer.
The SCINTF buffer now contains the 6 bit source code and when ENB was a one also SCICOMPE is one to enable the Comparator (figure 3.9a) where SCINTF is compared with IEC.

DESTINATION AND M BITS ARRIVE

The Destination code and spare bits still have to be shifted into the SCINT register, but are not decoded and have no meaning for the P857E CPU. The SCT counter will reach position 15. The total sequence (Start, Source, Destination, spare bits is repeated until the Interrupt is reset by a command (e.g. SST).

As soon as BCI becomes inactive (high) and SCTCAN=0, SCTLD and SCTLDDL become zero again. SCINTFZON becomes zero to reset SCINTF and also SCICOMPE, disabling the SCINTF and selecting the IEC lines to the IECSEL lines (see figure 3.9a).

3.9.2 INTERRUPT ENCODING

Both Serial (SCINTF0-5) and Parallel (IEC 0-5) encoded interrupts have the same encode/interrupt level relationship (see Table 3.12).

PARALLEL ENCODING

The Parallel encoded interrupts are divided into 4 groups:

- group 0, ints 0-7, when active indicated by INTGSON
- group 1, ints 8-15, when active indicated by INTGS1N
- group 2, ints 16-23, when active indicated by INTGS2N
- group 3, ints 24-31, when active indicated by INTGS3N

The groups are linked by enable signals (INTE0, 1, 2N) and when no interrupts are active then all 3 signals are active low.

EXAMPLE PARALLEL ENCODING

Consider the example of Figure 3.9A when it level 9 is active signal INTE1N indicates that the 2 lower groups (16-31) are inhibited. The 3 least significant bits (IEC 3, 4, 5) are encoded from the interrupt lines and the most significant bits (IEC 0, 1, 2) from the group indicator (in this example INTGS1N active). Level 9: IEC Ø, 1, 2, 3, 4, 5 = ØØ1ØØ1.

SERIAL ENCODING

The Serial Encoding takes place during the time a serial interrupt (BCI) is received (see 3.9.1).

EXAMPLE SERIAL ENCODING (FIGURE 3.9A/B)

The interrupt is received in a serial format (BCI, level 20) and is assembled as a 6 bit code in the D type F/Fs.

3.9.3 COMPARE PARALLEL/SERIAL (FIGURE 3.9A)

At the beginning of the CPU cycle (AP) both serial and parallel interrupts may have been received so the Serial (SCINTF 0-5) and Parallel (IEC 0-5) lines must be compared to find which has the highest encoded level. The result of this comparison is indicated by signal AGBO as follows:

- AGBO = 1 enable IEC lines (see example figure 3.9A)
- AGBO = 0 enable SCINTF lines

3.9.4 SELECT PARALLEL OR SERIAL ENCODES

The selection of the parallel or Serial encodes is made by signal AGBO as indicated above to enable the encoded interrupt level onto the IECSEL 0-5 lines.

3.9.5 COMPARE NEW INTERRUPT WITH CURRENT LEVEL

The current CPU interrupt level is on the PLR 0-5 lines. Two magnitude comparators (type LS85) are connected is cascade; the 4 least significant bits are handled first followed by the 2 most significant bits. The technique used to compare the new interrupt with the current level is shown in Figure 3.9C where the new interrupt level is 9 and the current level is 15.

The Interrupt Enable/Inhibit is handled at the same time as the comparison of the most significant bits. Signal ENBN (input A2) is compared with input B2 which is held at OV. When ENBN =1 (inhibit interrupts) the output A less than B is always 0 but when ENBN =0 the output A less than B depends on the cascading inputs (see Figure 3.9C). If the new interrupt is valid, IR =1 is generated.

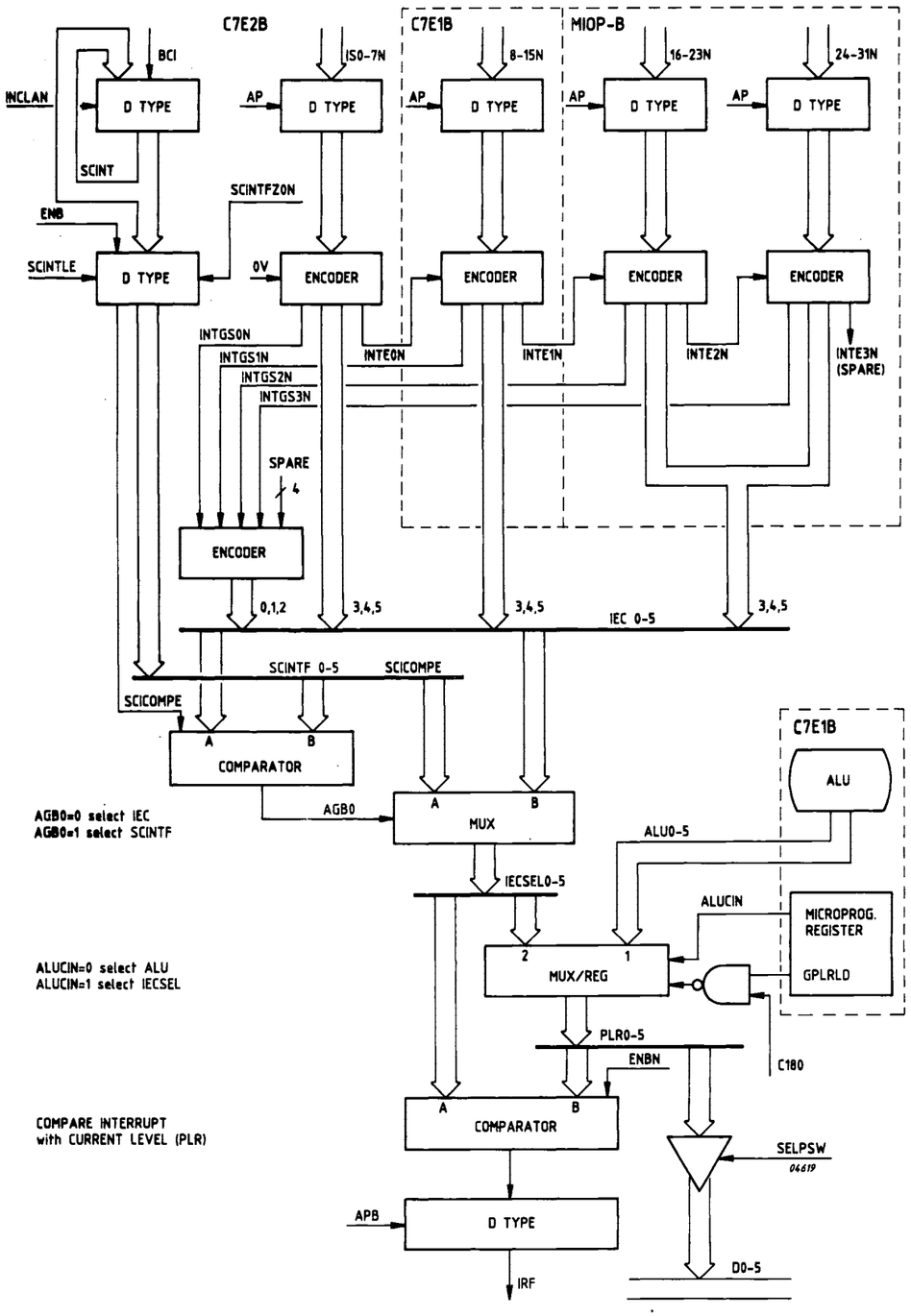
3.9.6 UPDATE PLR

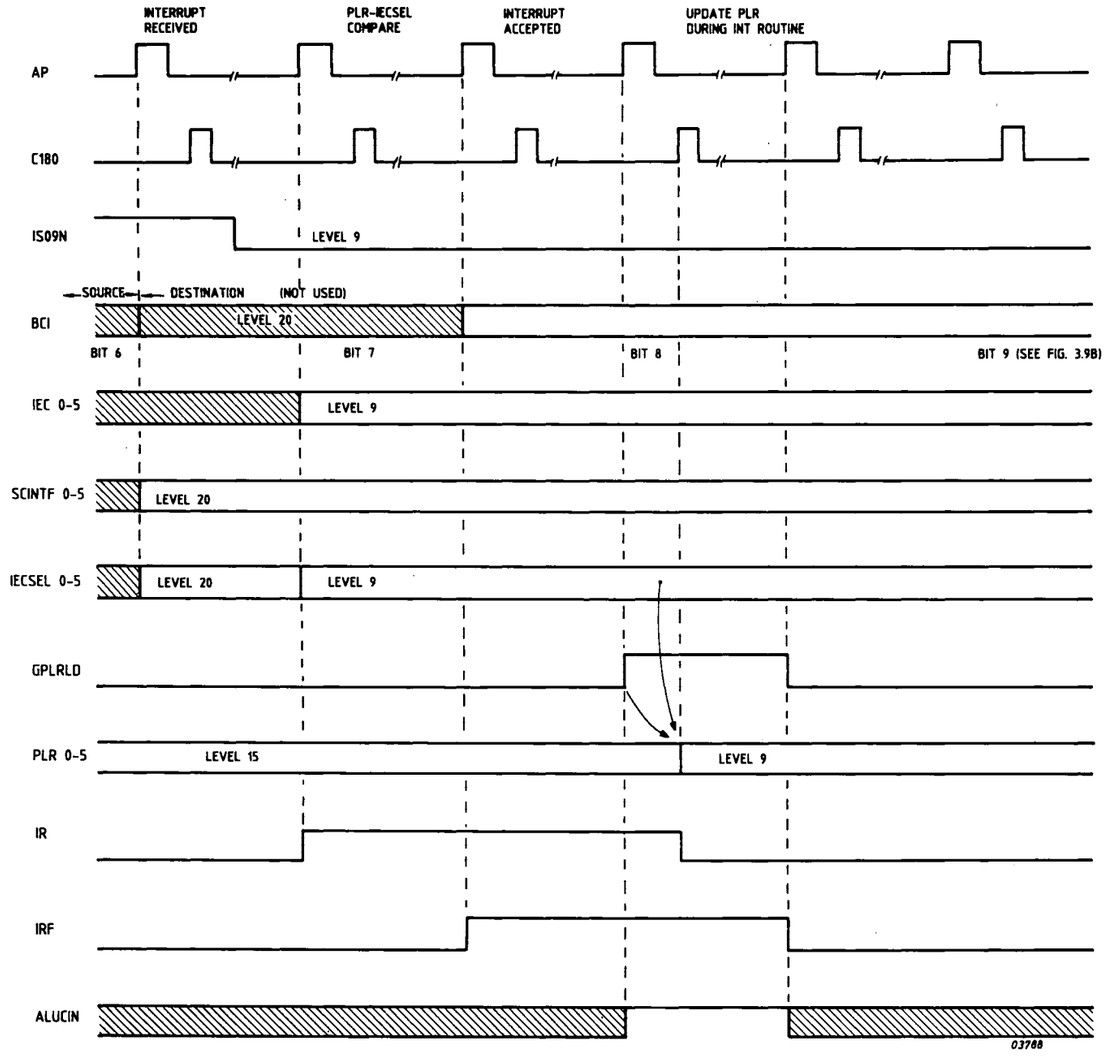
Signal IR =1, so at the beginning of the next CPU cyle signal APB clocks and validates IRF =1. Microprogram signal ALUCIN =1, so the value on the IECSEL lines (in this example level 9) is routed to the PLR during the interrupt micro-program routine generating GPLRLD signal.

Encoded Lines	Interrupt
0 1 2 3 4 5	Level
0 0 0 0 0 0	0
0 0 0 0 0 1	1
0 0 0 0 1 0	2
0 0 0 0 1 1	3
0 0 0 1 0 0	4
0 0 0 1 0 1	5
0 0 0 1 1 0	6
0 0 0 1 1 1	7
0 0 1 0 0 0	8
	9
	10
	11
	12
	13
	14
0 0 1 1 1 1	15
0 1 0 0 0 0	16
	17
	18
	19
	20
	21
	22
0 1 0 1 1 1	23
0 1 1 0 0 0	24
	25
	26
	27
	28
	29
	30
0 1 1 1 1 1	31
1 0 0 0 0 0	32
	33
	34
	35
	36
	37
1 1 1 1 1 1	63

Note 1: Interrupt level may be serial or parallel.

Table 3.12 ENCODE/INTERRUPT LEVELS





NOTE: TWO INTERRUPTS ARE RECEIVED (LEVEL 9 AND 20)
ONLY ONE LEVEL IS HIGH ENOUGH TO BE ACCEPTED

FIGURE 3.9A
INTERRUPT SYSTEM OPERATION P857E

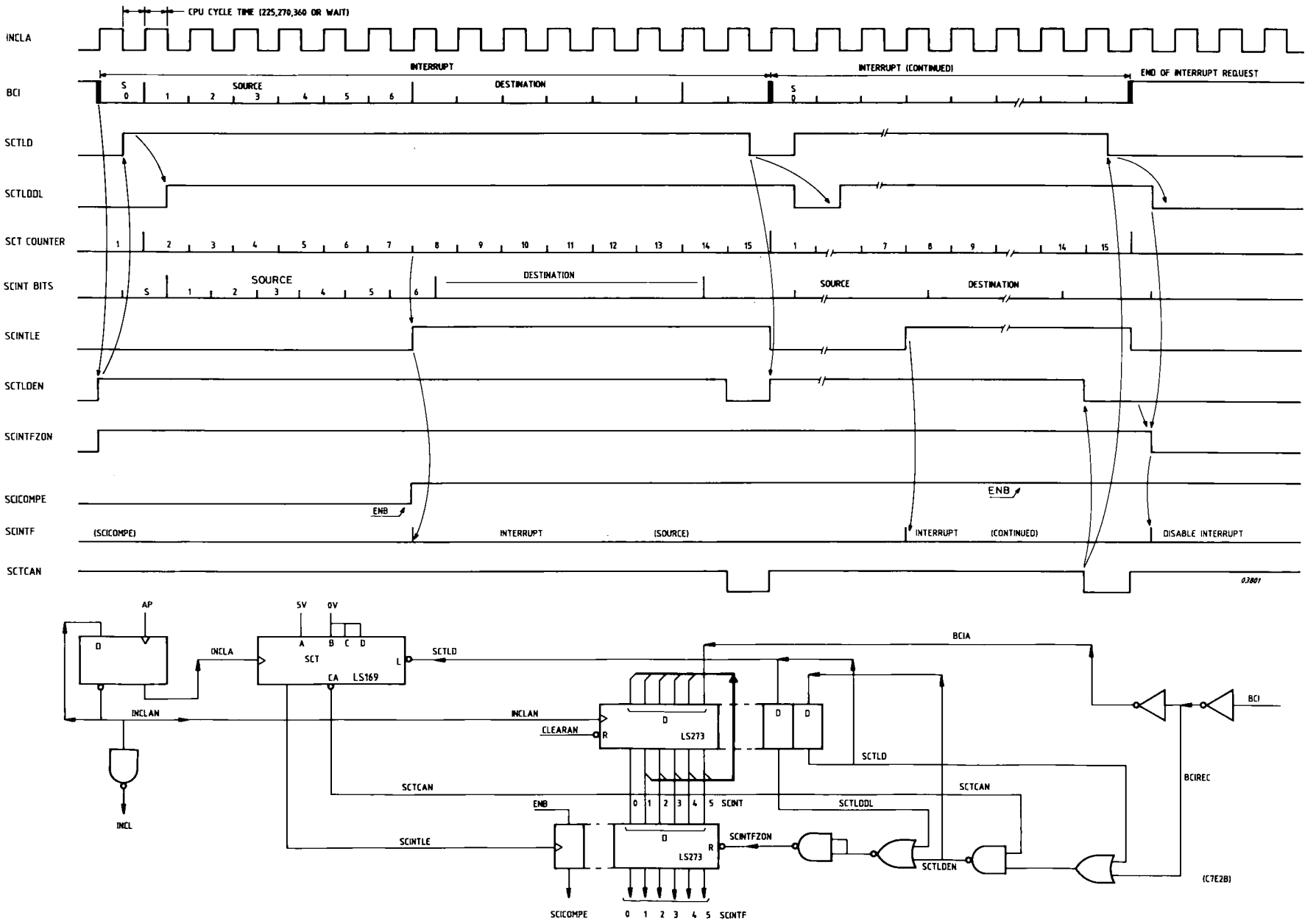
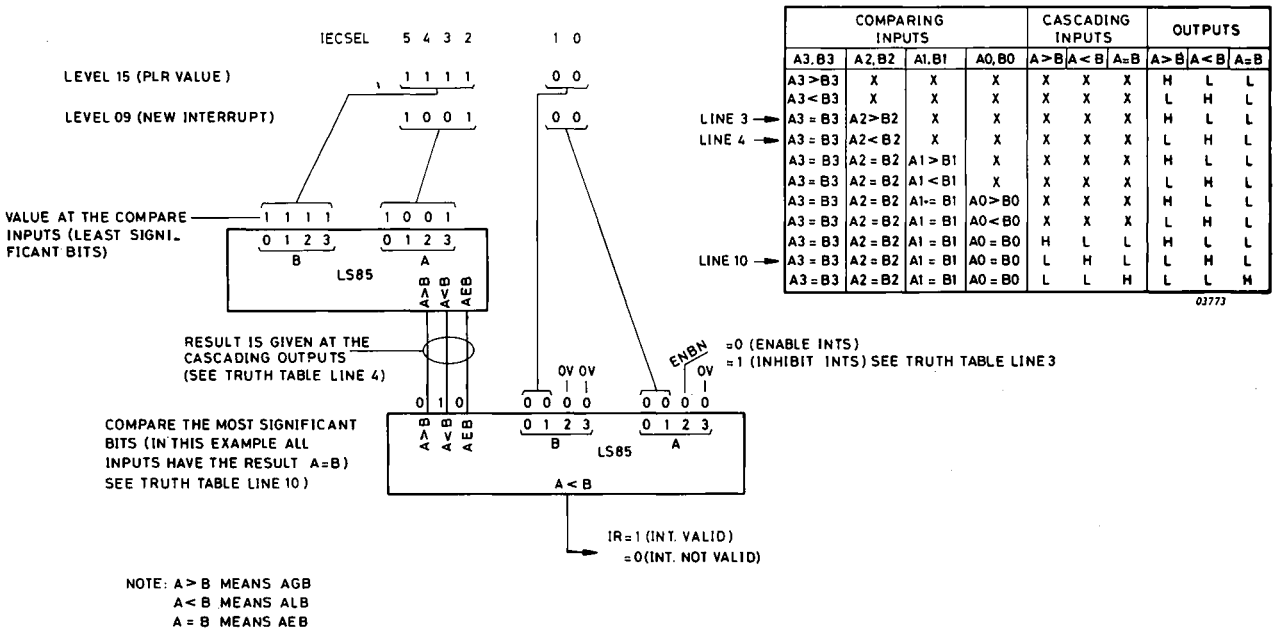


Figure 3.9B SERIAL INTERRUPTS ENCODING



	COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
	A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	A>B	A<B	A=B
	A3>B3	X	X	X	X	X	X	H	L	L
	A3<B3	X	X	X	X	X	X	L	H	L
LINE 3 →	A3=B3	A2>B2	X	X	X	X	X	H	L	L
LINE 4 →	A3=B3	A2<B2	X	X	X	X	X	L	H	L
	A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
	A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
	A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
	A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
	A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
LINE 10 →	A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
	A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H

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Figure 3.9C COMPARE NEW INTERRUPT WITH CURRENT LEVEL

3.10 CPU BUS CONTROL (FIGURE 3.10)

The Principles of Bus Control are already given in Chapter II. For purposes of this description the UPL Bus Operation is described as follows:

- CPU takes the Bus
- IOP requests the Bus

3.10.1 CPU TAKES THE BUS

The CPU takes the Bus under the following condition:

- Data Transfer (DE)

The CPU must inform the MIOP Function that it has taken the Bus with the following signals:

- BSYCPUEXN = 0 indicates that an MMU operation (Translation Mode) is to be carried out.
- BSYCPUN = 0 indicates that the CPU is busy with the Bus.

When the CPU is in the Bus cycle (Wait cycle) it must wait until TSMN is received. During this waiting period if the IOP or another Master requests the Bus (BUSRN) that Master will be allocated the Bus (MSN) but must wait until the CPU is no longer Busy with the Bus (BSYN = 1).

3.10.2 IOP REQUESTS THE BUS (FIGURE 3.10)

The IOP Function is considered as 2 Masters; IOPA and IOPB. Either one of these IOP's may request the Bus under the following conditions:

- ENBIOP = 1 to enable the generation of BUSRN.
- MSN = 1 no other Master is selected for a transfer.

If we consider the example of Figure 3.10 a Controller of IOPB is ready for a transfer (BR1ON is active, see MIOP/A). Signal BUSRQE enables a Bus Request BUSRN (IOP) which is received by the CPU Bus Controller and initiates the "search for requesting Master" procedure (C7E2/F).

The CPU Bus Controller will send OKO (after delay-time) to the first Master (IOPA). For this example (BR1O active) blocks the OKO chain at IOPB (BRGS1N =0; OKOBENB =0, see MIOP/G).
As soon as OKO/OKIA, OKOA/OKIB is received the Master (IOPB) is selected (MSN =0). MSN is sent to all Masters and cancels the signals BUSRN and OKO, OKOA.

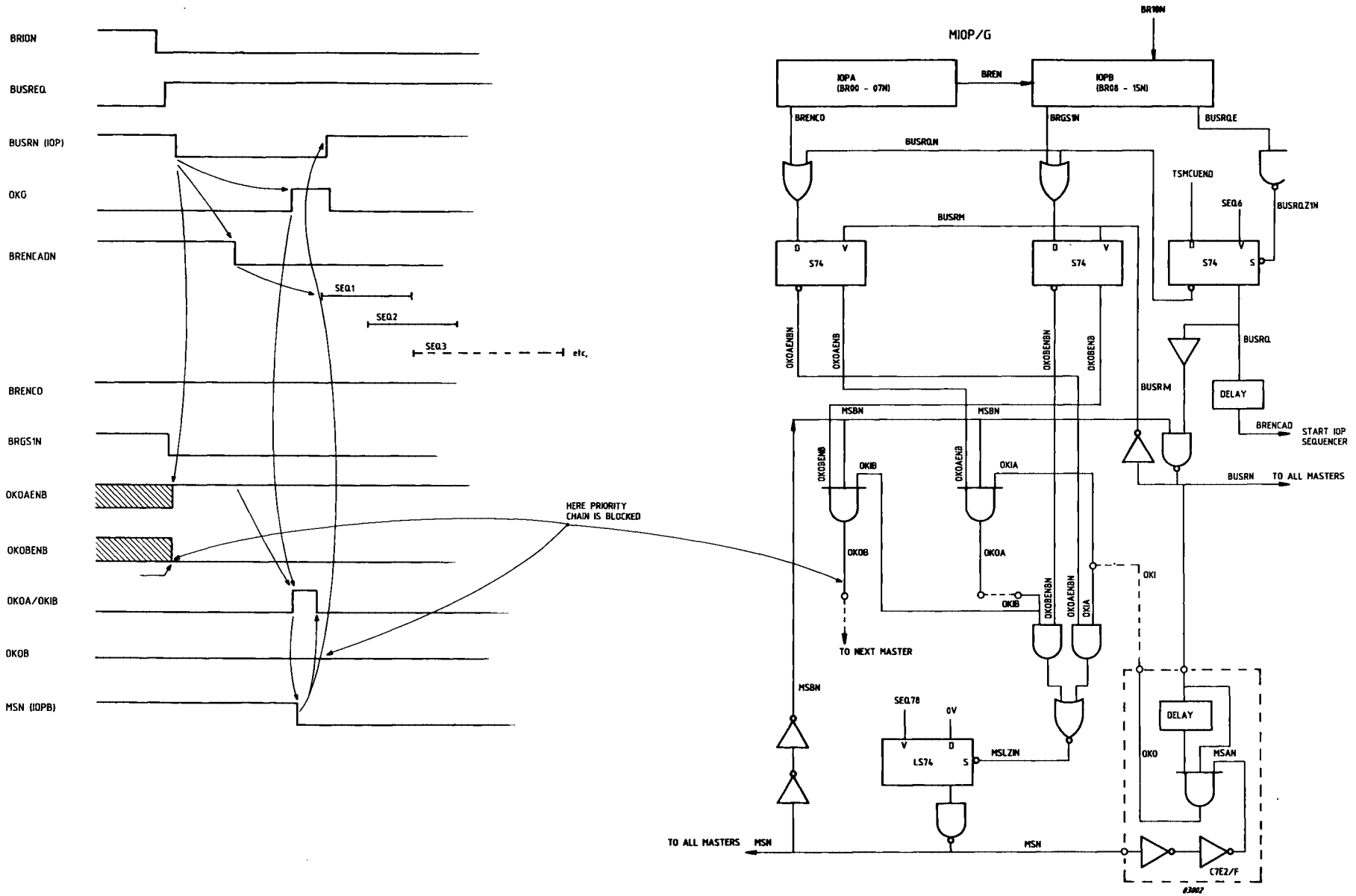


Figure 3.10 UPL BUS CONTROL

3.11 SERIAL INTERFACES (FIGURE C7E2/A AND FIGURE 3.11)

The principles of operation of the serial interfaces are explained in Chapter II. For purposes of this description the Control Logic is described in 3 parts:

- Common Control Logic
- V24 Interface Operation
- Control Panel Interface Operation.

The principal components used by the serial interfaces are:

- 8251A - this device is responsible for the serial/parallel conversion and buffering of data.
- COM5016 - this device supplies a constant frequency for the Control Panel Interface and enables a strap selectable frequency for the V24 Interface.
- 8304B - this device forms the interface between the ALU and DT lines.

3.11.1 COMMON CONTROL LOGIC (FIGURE 3.11A)

The Common Control Logic has the following functions:

- Indicate to the serial interface whether Control (NAD10 = 1) or Data (NAD10 = 0) is to be transferred on the 8-bit Bus.
- Select either the V24 or Control Panel interface with signals SEL8251N active, NAD03 = 0 (Control Panel), NAD3 = 1 (V24).
- Inhibit 2901 operation (NAD05 = 0).
- Validate data for Read (NAD08 = 0) or Write (NAD09 = 0) between the DT and ALU lines.

3.11.2 V24 INTERFACE OPERATION (FIGURE 3.11A-E)

The V24 interface enables an Operator Console to be connected to the P857E system. The peripheral commands are the standard commands associated with P800 (OTR, INR, SST, TST, CIO Halt) but the device address must always be /10. (Figure 3.11B-D).

INITIALISATION

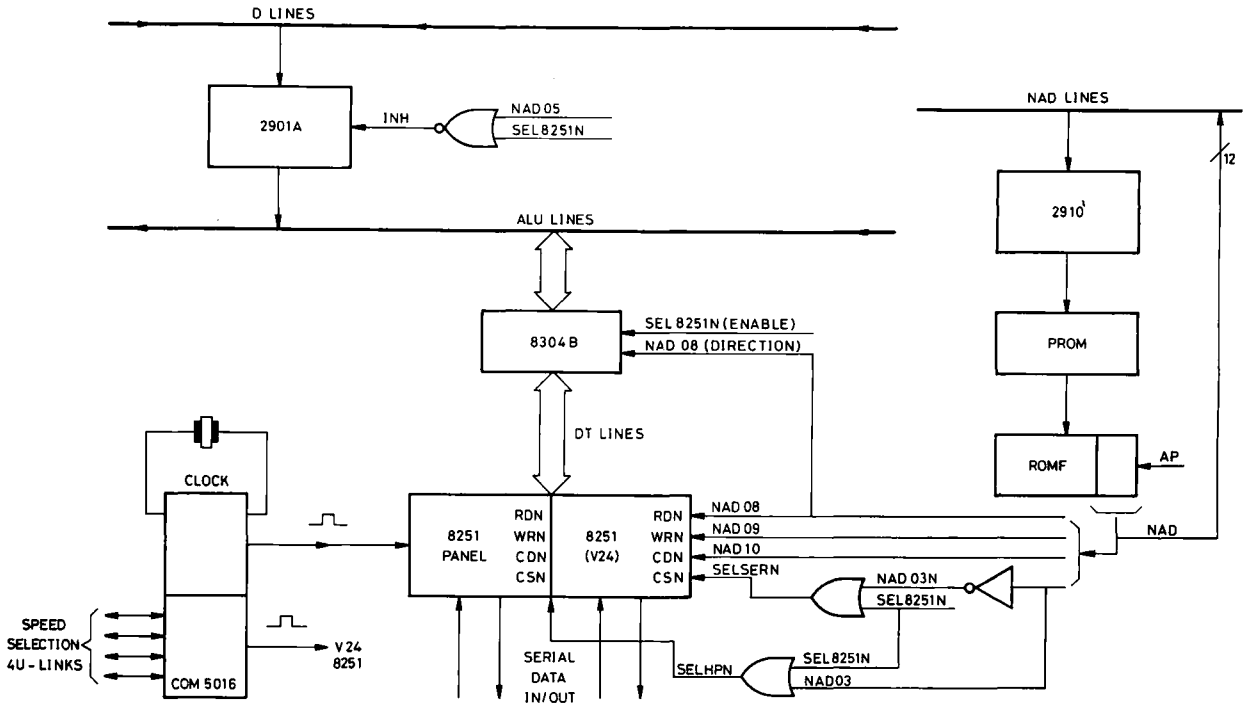
The V24 Interface (8251) is initialised with a Mode Instruction from the CPU for the following events:

- At Power-on time (RSLN)
- Whenever the Control Panel Interface (8251) generates the system Master Clear (CLEARN)
- During CIO commands after an internal reset.

V24 INTERRUPT (DIAGRAM C7E2/A)

The V24 Interface Interrupt INTSERN is generated for the following conditions:

- IN - when a character is deserialised signal INTREAD is active to enable INTSERN. DATA in 8251 is ready to go to memory by an INR instruction.
- ECHO - signal TXE indicates that the Transmitter is empty when the character is retransmitted. INTSERN is generated by INTREADA.
  Signal ECHO is one during Echo mode to inhibit the signal INTSERA. Otherwise INTSERN would stay active after an INR.
- OUT - signal INTWRITE is active when the last bit of the serialised character is transmitted to enable INTSERN which requests the next character. DATA can be stored in 8251, which can be done by an OTR instruction.
- WST - a PRE-WAIT state is written into the 8251 by the CIO Stop Command and signals INTWSTN=0, ECHO=1 are active. At the end of transmission of the last character signal TXE is active to enable INTSERN.



SELECT OPERATION

	CDN	RDN	WRN	CSN
CONTROL (CPU → 8251)	1	1	0	0
CONTROL (8251 → CPU)	1	0	1	0
DATA (CPU → 8251)	0	1	0	0
DATA (8251 → CPU)	0	0	1	0
DATA BUS - 3STATE	X	X	X	1
DATA BUS - 3STATE	X	1	1	0

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CDN = CONTROL OR DATA
CSN = CHIP SELECT
RDN = READ CYCLE
WRN = WRITE CYCLE

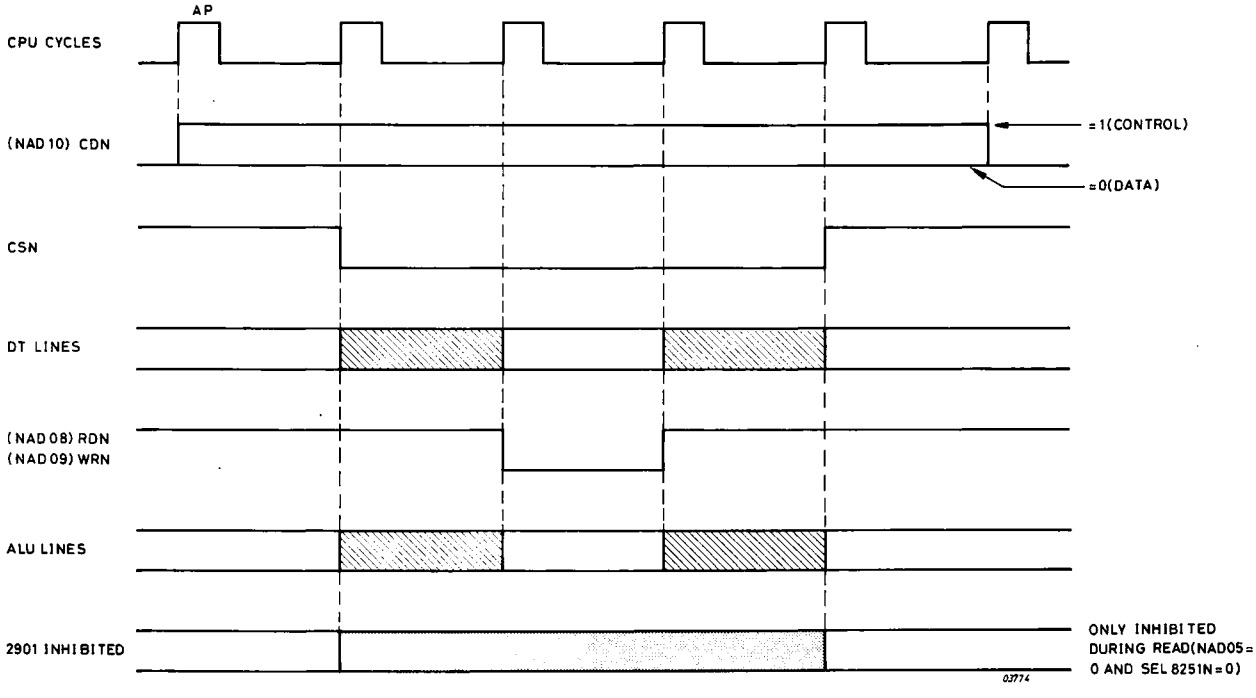


Figure 3.11A SERIAL INTERFACES - COMMON CONTROL LOGIC

V24 State Register (Figure 3.11D, E and C7E1/E)
The V24 State Register comprises 4 74LS173 F/Fs which are clocked during the CPU cycle by signal APC. The V24 Interface Micro Program writes into the State Register via the ALU lines and the Micro Program reads this state via the 2901 from the D-bus.

Pin no.	8251A Name	P857E Name	Description
9 25	TCN RCN	TRCPSN TRCPSN	Basic clock for the transmission and reception of serial data.
22	DSN	CT107N	Modem Ready signal sets an internal 8251A F/F. This condition is read by the Read Status Command.
11	CSN	SELSERN	Select V24 interface, enabled with SEL8251N active and NAD03 = 1.
17	CTN	CTSN	Link selection (CT133); either holds CTSN permanently at OV or CT133 enables CTSN when the device is ready. CTSN enables serial transmission when Command Bit TxEN = 1.
20	CLK	SERCL	Derived from the CPU Clock to form the basic timing for the Read/Write cycles.
13	RDN	NAD08	Active low from the CPU to indicate that the 8251A must place either data or status on the data lines.
10	WRN	NAD09	Active low from the CPU indicates to the 8251A that data or a Control Word is waiting on the data lines.
12	CDN	NAD10	From the CPU and used in conjunction with RDN and WRN to enable either Control or Status at the Data Bus (high) or Data (low).
21	RES	CLEAR	From the 8251A (Control Panel) after a Master Reset which resets the 8251A (V24).
3	RXD	CT104N	Serial data received by the 8251A from the Peripheral.
18	TXE	TXE	Transmitter empty, active high indicates that the 8251A has transmitted a character from its buffer. (During transmission of a character TXE low inhibits interrupt INTSERN).
23	RTN	INTWSTN	After a CIO Stop this indicates the Pre-Wait state; at the end of the last character TXE enables the WST interrupt.
14	RDY	INTREAD	Receiver Ready indicates that the Receiver Buffer has a character ready.
15	TDY	INTWRITE	Transmitter Ready, active high indicates that the Transmitter is ready to accept the next character.

Table 3.13 8251A (V24) PIN DESIGNATIONS

Pin no.	8251A Name	P857E Name	Description
24	DTN	ECHO	The Command instruction sets the 8251A internal F/F so that ECHO is active high during Echo Mode or Low if no Echo Mode.
19	TXD	CTIO3N	Serial data from 8251A to the device.
16	SYN	BREAK	For Input mode when the Break Key is pushed it generates an all zero character which is recognised as an interrupt request. BREAK goes high to enable the interrupt.
27	D0	DT15)	8-bit, 3-state, bi-directional buffer lines to interface the 8251A to the CPU. These lines may contain data, status or control information depending on the condition of the 3 control lines RDN, WRN, CDN.
28	1	14)	
1	2	13)	
2	3	12)	
5	4	11)	
6	5	10)	
7	6	09)	
8	7	08)	

Table 3.13 8251A (V24) PIN DESIGNATIONS (CONT'D)

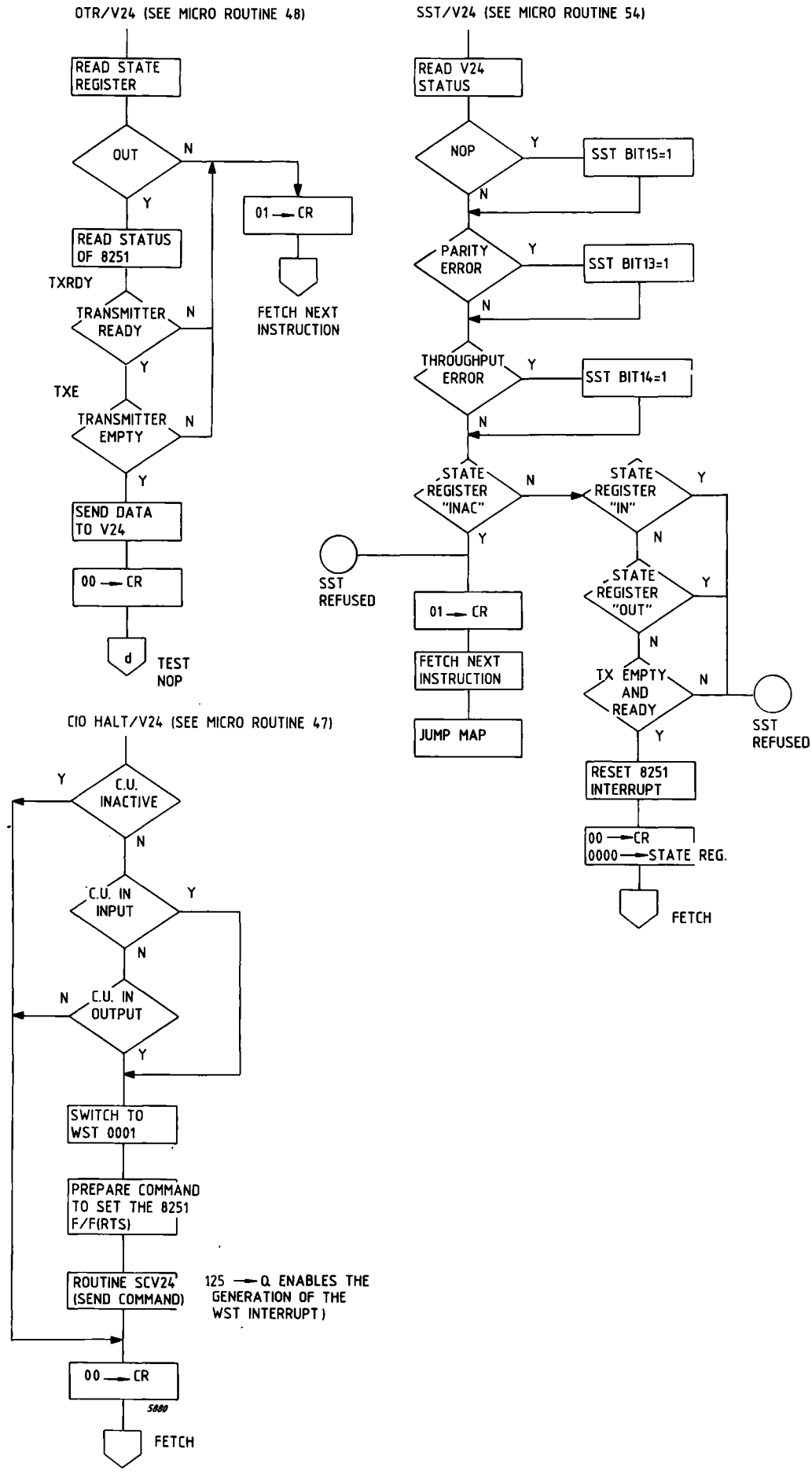


Figure 3.11B OTR/V24, SST V24, CIO HALT

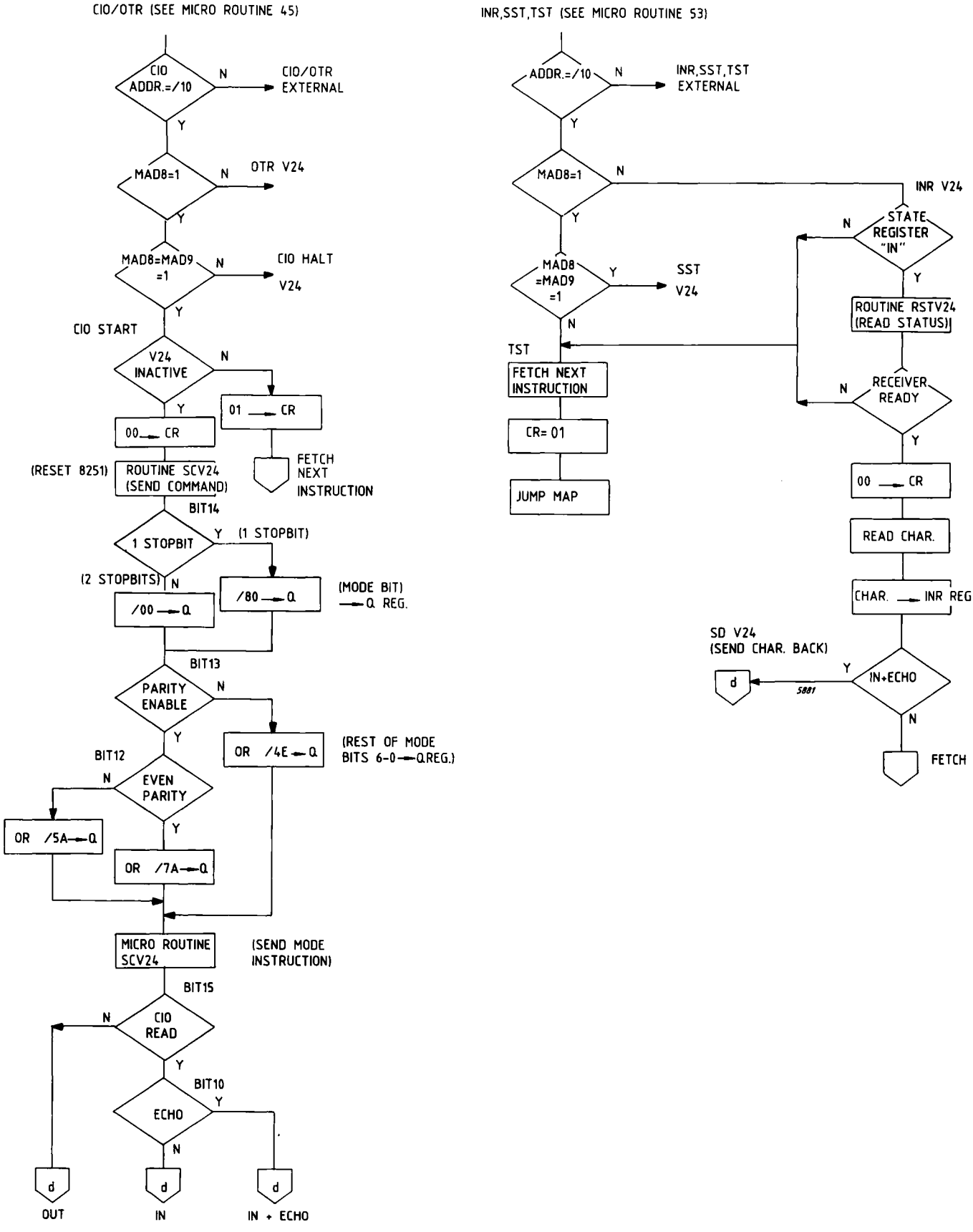


Figure 3.11C CIO/OTR, INR, SST, TST

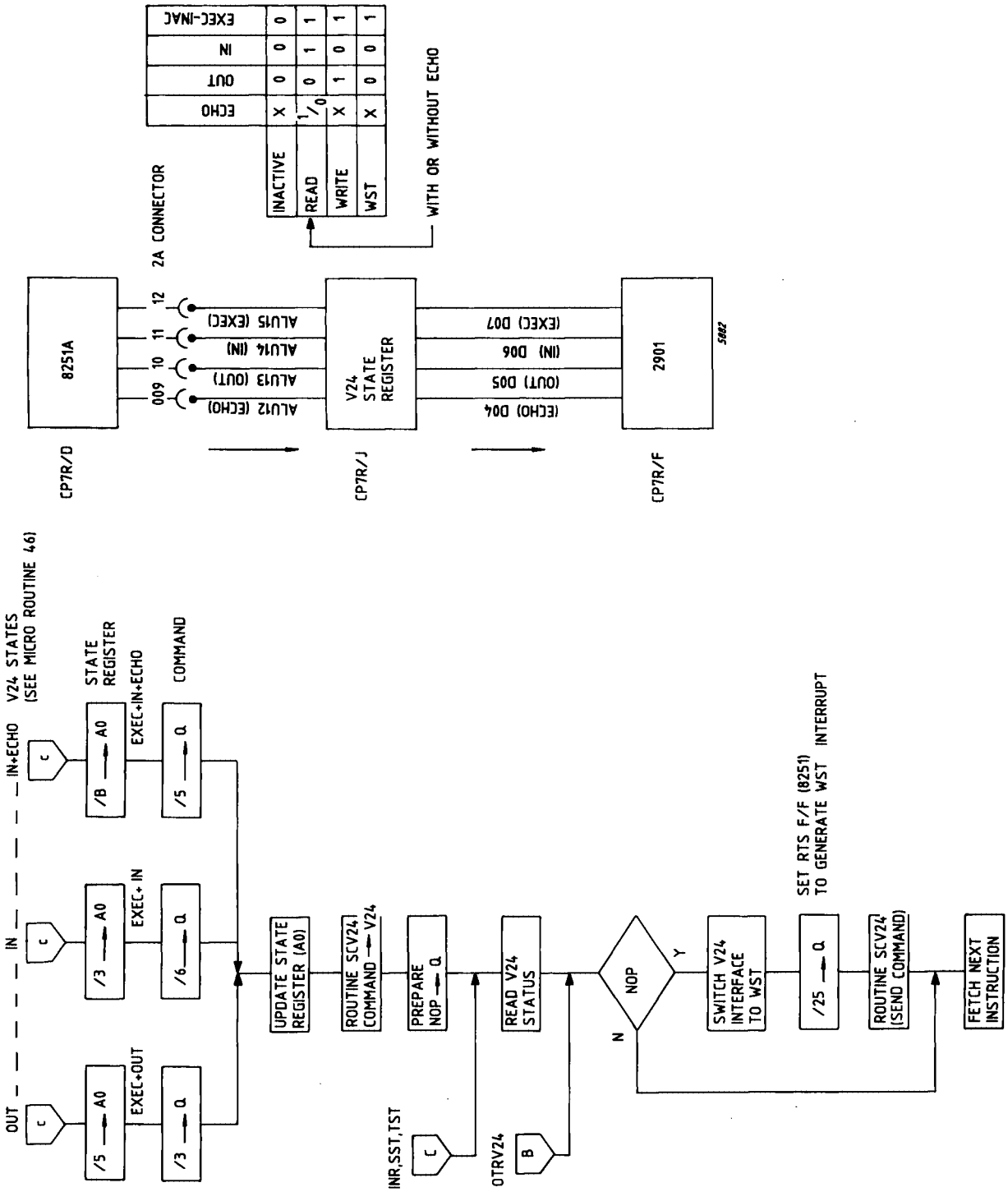
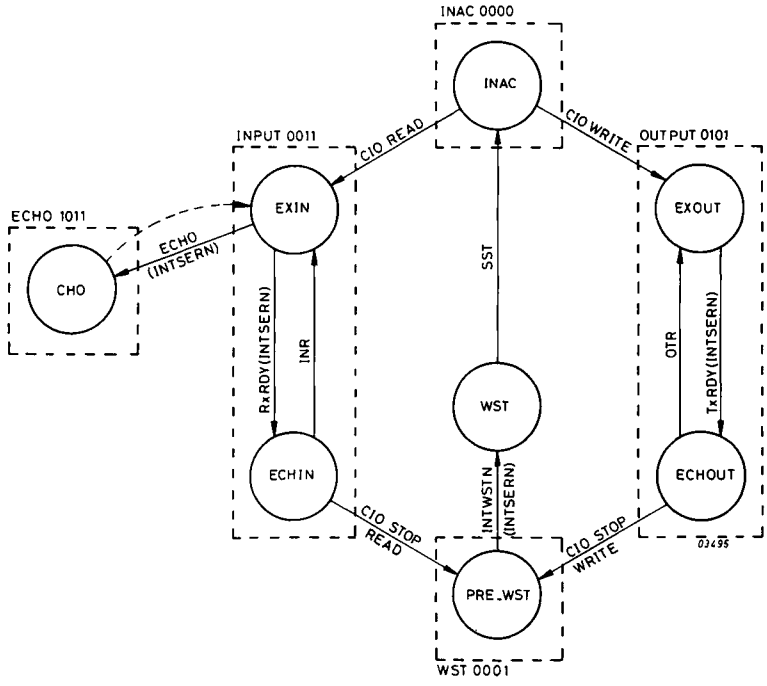


Figure 3.11D V24 STATES: OUT, IN, IN + ECHO



Note: The states of the V24 Interface have a different significance at the P857E level. Only INAC, OUTPUT, INPUT, ECHO and WST are read by the P857E V24 State Register.

Figure 3.11E V24 INTERFACE STATES

3.11.3 CONTROL PANEL INTERFACE OPERATION

The Control Panel Interface enables a serial control panel to be connected to the P857E system.

INITIALISATION (Figure 3.7)

The Control Panel Interface (8251) is cleared by RSLN and initialised with a Mode Instruction from the CPU whenever the system is powered on (RSL micro program).

CONTROL PANEL INTERRUPT

The Control Panel interrupt PUPHP is initiated from a Control Panel Function Button. The action of pushing the button simulates a character on the serial input line SDPM and when the 8251 Receiver Buffer is full signal PUPHP is active. This signal generates the signals PUPF and RUNIRN to the PLAMAP.

GENERATE SYSTEM MASTER CLEAR

The System Master Clear (CLEARN) is generated for the following events:

- Power-on time
- When the Control Panel MCL or IPL button is pressed and system is not in RUN mode.
- With IPL remote
- When Diagnostic test is started.

These events set the 8251 internal F/F DTR to enable signal CLEARA active and in turn generate CLEARN.

CONTROL PANEL MICRO-ROUTINES

When a character is received at the Control Panel Interface, the Microprogram is responsible for the decoding (Function, Data or Address) and the subsequent action; see Figure 3.11F.

OPERATOR ACTION

To show the working of the Control Panel Interrupt, consider that the operator has pushed data button "5" followed by function button "RR". The action of pushing the Function button causes the signal PUPHP to go active high because the 8251 (Panel) will receive something (C7E2/A). At this point the CPU stays in Idle Mode (/38D, 38E, 5F2, 604, 38D).

ADDRESS /38D

As there is a JMAP Micro-inst executed at this point, the PLAMAP input conditions are as follows:

- PUPF = 1
- IR = 0
- RUN = 0 so RUNIRN=1 and PUPFE=1

From the PLAMAP (Table 3.8) Product 01, the following address appears at the NAD lines:

NAD lines	0	1	2	3	4	5	6	7	8	9	10	11
Address (/3CD)	0	0	1	1	1	1	0	0	1	1	0	1

This address is the start of the Control Panel Routine (PUPITRE).

ROUTINE-CONTROL-PANEL/IPL/PRESET

At the entry of this routine the CPU does not know which of these conditions exist so this routine must determine whether or not it is the Control Panel by testing the 8251 (Control Panel) Buffer Status bit RxRDY. The 2932 PC must be even during these operations and so bit 15 is systematically put to 0.

ADDRESS /3CD, /3CE, /5DE

The 2932 PC, bit 15 is zeroed by executing a shift right (AOSHR) and then a shift left (AOSHL).

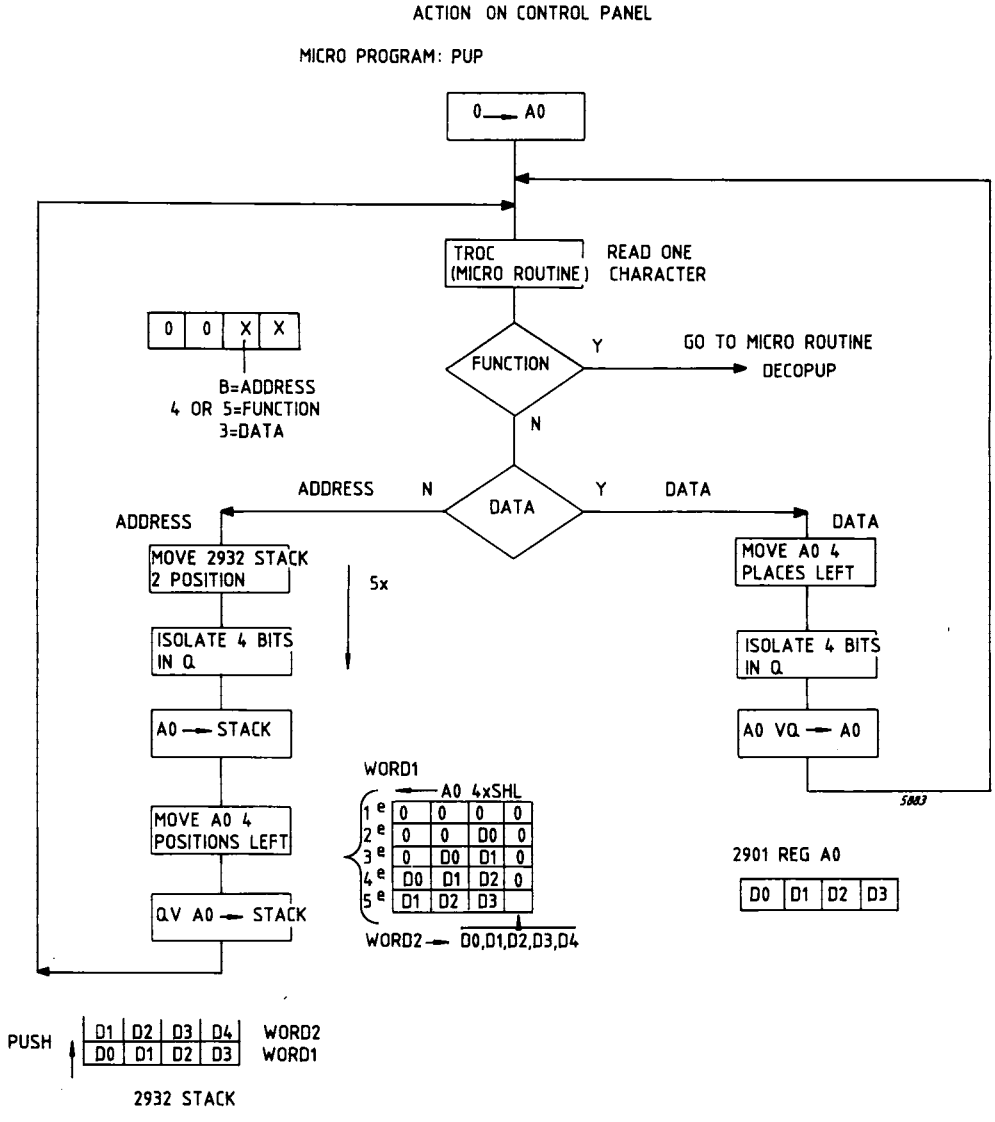


Figure 3.11F CONTROL PANEL SENDS CHARACTER

Pin no.	8251A Name	P857E Name	Description
9 25	TCN RCN	TRCPHN TRCPHN	Basic clock for the transmission and reception of serial data.
22	DSN	LOCK	From the Control Panel LOCK switch this signal sets an internal 8251A F/F which is read by the Read Status Command.
11	CSN	SELHPN	Select Control Panel Interface, enabled with SEL8251N active and NAD03 = 0.
17	CTN	0V	Held at 0V to enable serial transmission when Command Bit TxEN = 1.
20	CLK	SERCL	Derived from the CPU Clock to form the basic timing for the Read/Write cycles.
13	RDN	NAD08	Active low from the CPU to indicate that the 8251A must place either data or status on the data lines.
10	WRN	NAD09	Active low from the CPU indicates to the 8251A that data or a Control Word is waiting on the data lines.
12	CDN	NAD10	From the CPU and used in conjunction with RDN and WRN to enable either Control or Status at the Data Bus (high) or Data (low).
21	RES	RSLF	Derived from the Power Supply signal RSLN to reset the 8251A (Control Panel) which in turn enables the signal CLEARN to the system during the RSL micro program execution.
3	RXD	HPINPUT	This input receives serial data from the Control Panel if the Panel is not locked.
24	DTN	CLEARA	This is the output of the DTR F/F (internal to the 8251A) which enables the system reset CLEARN.
19	TXD	HPOUT	This output is the serial data to the Control Panel.
14	RDY	PUPHP	Control Panel Interrupt when a character has been received from RXD.
27 28 1 2 5 6 7 8	D0 1 2 3 4 5 6 7	DT15) 14) 13) 12) 11) 10) 09) 08)	8-bit, 3-state, bi-directional buffer lines to interface the 8251A to the CPU. These lines may contain data, status or control information depending on the condition of the 3 control lines RDN, WRN, CDN.

Table 3.14 8251A (CONTROL PANEL) PIN DESIGNATIONS

ADDRESS /5DE, /5DF, /5E0, /5E1

A mask is loaded into 2901 Register Q so that status bit 14 (RxRDY) can be tested. The status of the 8251 (RXRDY) is read at the same time and stored into the 2932 stack.

ADDRESS /5E2

The bit 14 value is tested using ALUZERO. If the test is true (as in this example) then the 2910 continues to address /5E3. If the test is not passed a CJP takes the Micro-Routine to Remote IPL/Preset. Bit 14 is fetched from 2932 stack, and compared with register Q bit 14.

ROUTINE - CONTROL PANEL (PUP, Figure 3.11F)

On entering the Control Panel Routine any of the following conditions may have initiated this action:

- a function by itself (e.g. POFF)
- 1 data character + function (e.g. RR)
- 4 data characters + function (e.g. LR)
- an address, 5 characters + function (e.g. LA).

This routine must identify the character and treat it accordingly. ASCII codes are used to identify the characters as follows:

- function is prefixed with 4 or 5
- address is prefixed with /B
- data is prefixed with 3.

After identification if it is either address or data then this must be stored as follows:

- an address of 5 characters is stored in the Stack of the 2932.
- 4 data characters are stored in the Register A0 of the 2901.

ROUTINE - TROC

During the Control Panel Micro-Routine the sub-routine TROC was used to read one character from the 8251 (Control Panel) and load it into 2901 register Q. This routine may be considered as 2 separate parts:

- Addresses /5AD to /5B1
  Here the status of the 8251 is read to ensure that data is ready (RxRDY=1). If RxRDY=0 then the routine loops until data is ready.
- Addresses /5B2 to 59F
  Here the character is read and placed in Register Q.

In this example push button RR is pressed so there is a function in the form of 4x or 5x (for RR code /42). The functions are decoded by the routine DECOPUP. Before this function the charater /35 (Data Button "5") was received.

ROUTINE DECOPUP; ADDRESSES /020 ONWARDS

Here the function code is tested by a series of shift right's (SHR). In the example of RR the exit from this routine is at address /571 and continues to /572. The data character was saved in ALUX (/020).

ROUTINE - READ REGISTER

This routine will display the contents of Register A5 (selection is in ALUX).

ADDRESSES /572 TO /579

To ensure compatibility with the R1 Field these addresses are responsible for repositioning the bits as follows:

Test most significant bit of register selection (A0 bit 4). This bit will be put at position 8 of register A0 of the 2901. Also A0 bit 0 will be set to indicate no T8 type of instruction. Now in word /579 R1 can be loaded from D-bus bit 5678. Bit 8 is in fact the most significant (8567).

ADDRESSES /57A ONWARDS

The R1 value is 5 which points to a 2901 register. When the R1 value is 0 then this is the PC which is in the 2932 so at address /57A a test is made to establish if it is reg A0 or not.

3.12 INITIAL PROGRAM LOADER (FIGURE 3.12)

The Initial Program Loader (IPL) is contained in a 1K x 4-bit ROM (C7E2/B). The IPL routine is responsible for loading the Bootstrap into Memory at Initiation time. Initiation can be in one of 3 ways:

- at switch-on, if the Control Panel is in the LOCK position and the Battery has been off.
- from a Remote Device.
- from the Control Panel IPL Button.

A Micro-Routine BOOT controls the loading of the Bootstrap ROM 1k x 4-bits into the Memory Stack in a 256 x 16-bit format.

3.12.1 BOOTSTRAP ROUTINE (MICROPROGRAM NO. 8)

The Bootstrap Routine uses the 2932 as follows:

- Program Counter (PC) as the Quartet counter for the ROM addressing.
- Register R (R) as the word counter for the RAM Memory.

This routine assembles the ROM quartets into 16-bit words and then loads 256 words into the Memory. The contents of the panel display was stred in A15 before the Bootstrap routine is started (/18B).

3.12.2 AUTO OR REMOTE IPL ROUTINE (MICROPROGRAM NO. 8)

This Routine enables one of the last 16 words of the Bootstrap to be read. A value (/0-/F) is read from the OPSO-3N lines and added to decimal 240. This value is now loaded into MADS to address the appropriate word in the Memory. The contents of this memory address overwrites the contents of A15.

3.13 MICRODIAGNOSTIC (FIGURE 3.13)

At Power-On time an Automatic Test is carried out (see Figure 2.2), if this test is passed then code /FFFC is displayed at the Control Panel so now the Microdiagnostics may be carried out (Figure 2.3). The Microdiagnostic test is initiated by the operator from the Control Panel Button TEST together with 0.

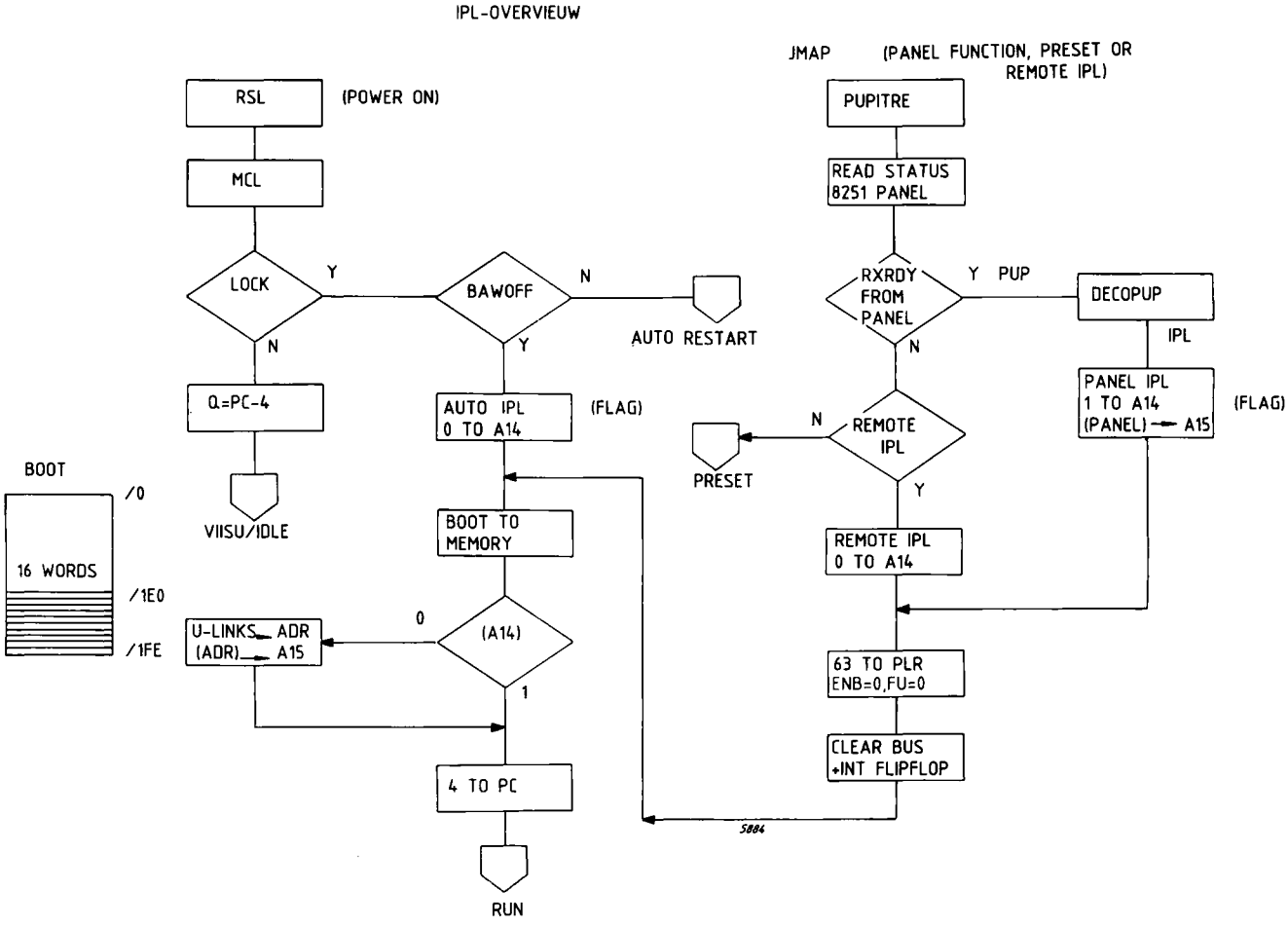


Figure 3.12 IPL PRINCIPLE OF OPERATION

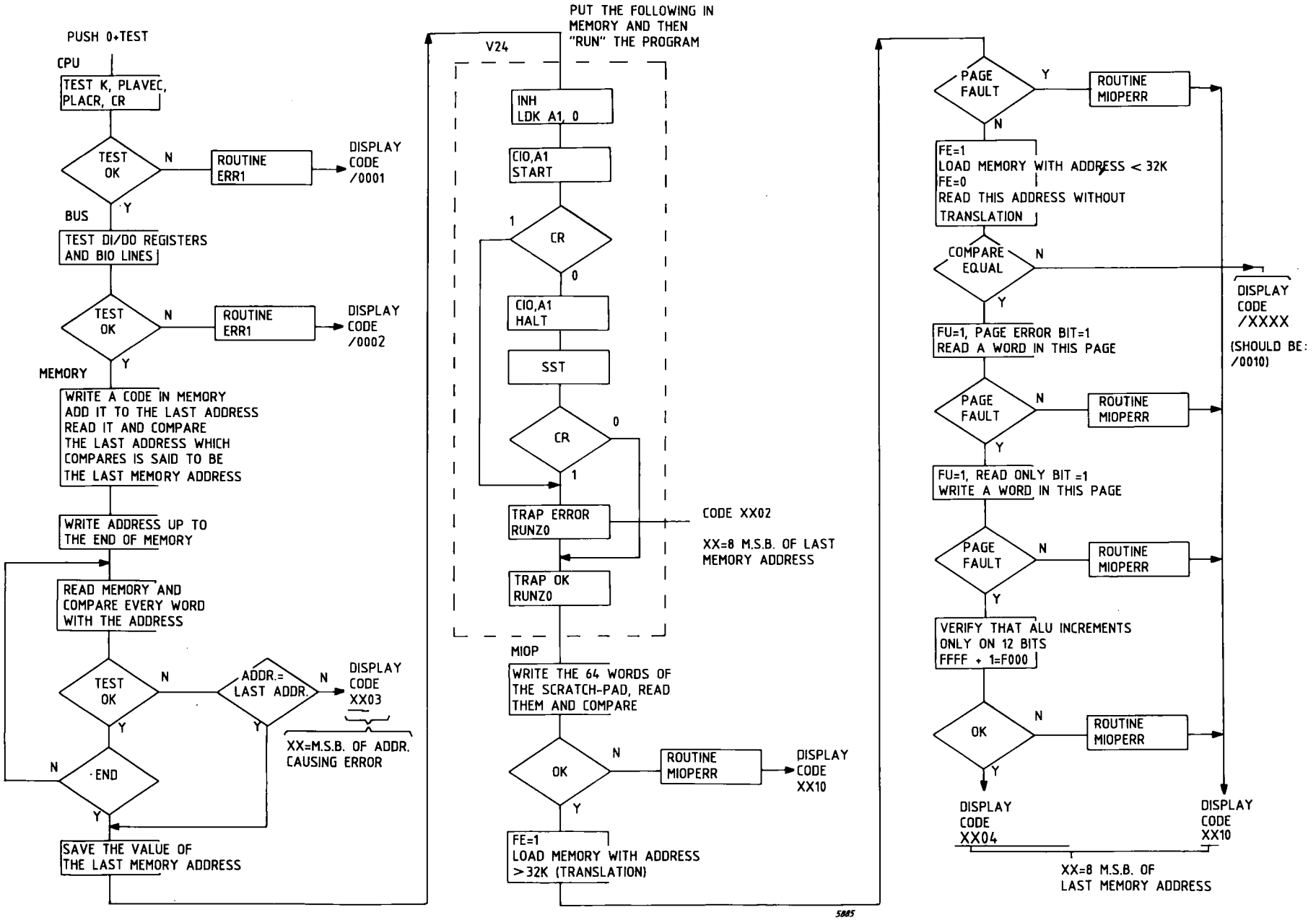


Figure 3.13 MICRODIAGNOSTICS - PRINCIPLE OF OPERATION

3.14 PROGRAM STATUS WORD (FIGURE 3.14)

The Program Status Word (PSW) is a 16-bit word which indicates the machine state after certain operations have been carried out. These operations are as follows:

- Interrupt
- Trap
- Page Fault
- Call Function
- Halt
- Inhibit Interrupt
- Reset Internal Interrupt
- Enable Interrupt
- Link to Monitor
- Set Mode

As a result of some of these operations the PSW is saved in the Stack under Microprogram Control ready for a return (RTN). For a Return the restoring of the PSW depends whether the RTN is a RTN A15 or a RTN A1-A14. For RTN A15 the following are restored:

- Program Level Register (PLR)
- Condition Register (CR)
- ENB, FE and FU bits of the General F/Fs.

For RTN A1-A14 only the CR is restored from the Stack. The principal components for writing the PSW onto the D lines are shown in Figure 3.14. Note that one half of the PSW (D00-D07) is written in true value whereas D08-D15 are inverted.

3.15 MIOP (FIGURE 3.15)

The MIOP Card has 4 functions (3.15A).

- Input/Output Processor (IOP) to multiplex up to 16 Control Units, addressing up to 8M words.
- Memory Management Unit (MMU) to extend the addressing capability up to 8M words (24 bits) and to provide page protection.
- Stop On Preset Address (SOPA) to stop on an address pre-loaded into a register, this facility addresses up to 512K words (20 bits).
- Interrupt Encoding Logic for parallel interrupts IS16N-IS31N (chapter 3.9).

The first 3 functions have certain operations that are common, so for purposes of this description these operations are summarised in the following par. Common Logic.

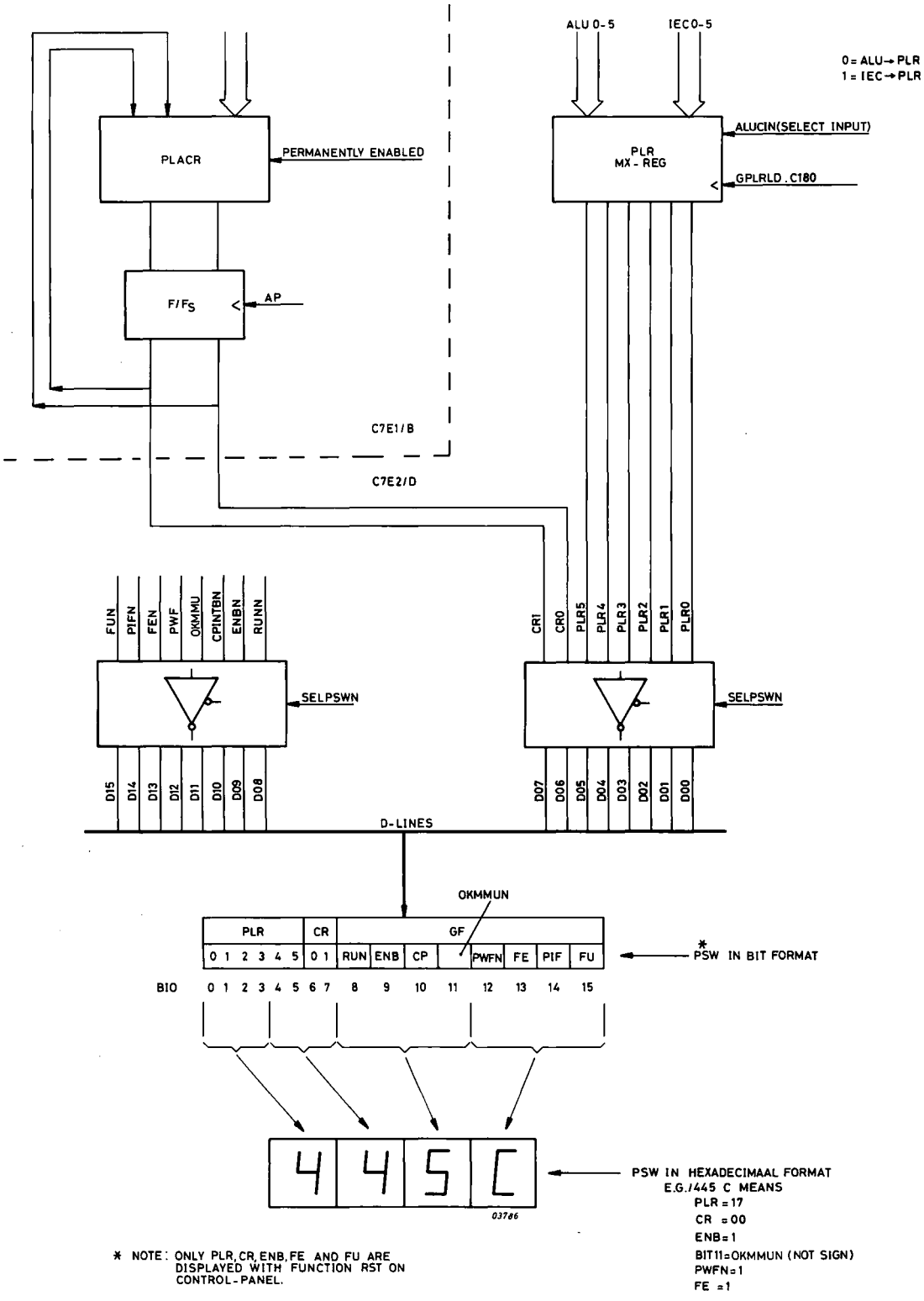


Figure 3.14 WRITE PSW TO D LINES

Pin No	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9	10	11	FUNCTION
	INPUTS																OUTPUTS		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6 5 4 3 2 1 0	
	ALU0X1	T1MEOUT	CR1	CR0	ACC	TPM	ALUZER	ALUSIG	AUV	AUO7	AUO6	FCRR1	FCRR0	PACR2	PACR1	PACR0	PLCR1	PLCR0	
STX																	H	H H H H H H H 34	
00	-	-	L	L	-	-	-	-	-	-	-	-	-	L	L	L	.	. . . . .	No change
01	-	-	L	H	-	-	-	-	-	-	-	-	-	L	L	L	.	A	No change
02	-	-	H	L	-	-	-	-	-	-	-	-	-	L	L	L	A	. . . . .	No change
03	-	-	H	H	-	-	-	-	-	-	-	-	-	L	L	L	A	A	No change
04	-	-	-	-	-	-	-	-	-	L	L	-	-	H	L	L	.	. . . . .	RTN
05	-	-	-	-	-	-	-	-	-	L	H	-	-	H	L	L	.	A	RTN
06	-	-	-	-	-	-	-	-	-	H	L	-	-	H	L	L	A	. . . . .	RTN
07	-	-	-	-	-	-	-	-	-	H	H	-	-	H	L	L	A	A	RTN
08	-	H	-	-	-	-	-	-	-	-	-	-	-	L	H	L	A	A	I/O Not recognised
09	-	L	-	-	L	-	-	-	-	-	-	-	-	L	H	L	A	. . . . .	I/O Not accepted
10	-	L	-	-	H	-	-	-	-	-	-	-	-	L	H	L	.	. . . . .	I/O Accepted
11	-	-	-	-	-	-	-	-	-	-	-	L	L	H	H	L	.	. . . . .	FPP
12	-	-	-	-	-	-	-	-	-	-	-	L	H	H	H	L	.	A	FPP
13	-	-	-	-	-	-	-	-	-	-	-	H	L	H	H	L	A	. . . . .	FPP
14	-	-	-	-	-	-	-	-	-	-	-	H	H	H	H	L	A	A	FPP
15	-	-	-	-	-	-	H	L	-	-	-	-	-	L	L	H	.	. . . . .	CRLOG Zero
16	-	-	-	-	-	-	L	L	-	-	-	-	-	L	L	H	A	. . . . .	CRLOG Positive
17	-	-	-	-	-	-	L	H	-	-	-	-	-	L	L	H	.	A	CRLOG Negative
18	-	-	-	-	-	-	L	L	L	-	-	-	-	H	L	H	A	. . . . .	CRAR Positive
19	-	-	-	-	-	-	L	L	H	-	-	-	-	H	L	H	A	A	CRAR Overflow
20	-	-	-	-	-	-	L	H	L	-	-	-	-	H	L	H	.	A	CRAR Negative
21	-	-	-	-	-	-	L	H	H	-	-	-	-	H	L	H	A	A	CRAR Overflow
22	-	-	-	-	-	-	H	L	L	-	-	-	-	H	L	H	.	. . . . .	CRAR Zero
23	-	-	-	-	-	-	H	L	H	-	-	-	-	H	L	H	A	A	CRAR Overflow
24	-	-	-	-	-	-	L	L	L	-	-	-	-	L	H	H	A	. . . . .	CR Compare greater
25	-	-	-	-	-	-	H	L	H	-	-	-	-	L	H	H	.	A	CR Compare smaller
26	-	-	-	-	-	-	H	L	L	-	-	-	-	L	H	H	.	. . . . .	CR Compare Zero
27	-	-	-	-	-	-	H	L	H	-	-	-	-	L	H	H	.	A	CR Compare Zero
28	-	-	-	-	-	-	L	H	L	-	-	-	-	L	H	H	.	A	CR Compare smaller
29	-	-	-	-	-	-	L	H	H	-	-	-	-	L	H	H	A	. . . . .	CR Compare greater
30	L	-	-	-	-	-	H	-	-	-	-	-	-	H	H	H	.	. . . . .	CR SLA or DLA Zero
31	H	-	-	-	-	-	-	-	-	-	-	-	-	H	H	H	A	A	CR SLA or DLA Overflow
32	L	-	-	-	-	-	L	L	-	-	-	-	-	H	H	H	A	. . . . .	CR SLA or DLA Positive
33	L	-	-	-	-	-	L	H	-	-	-	-	-	H	H	H	.	A	CR SLA or DLA Negative

Table 3.15 PLACR

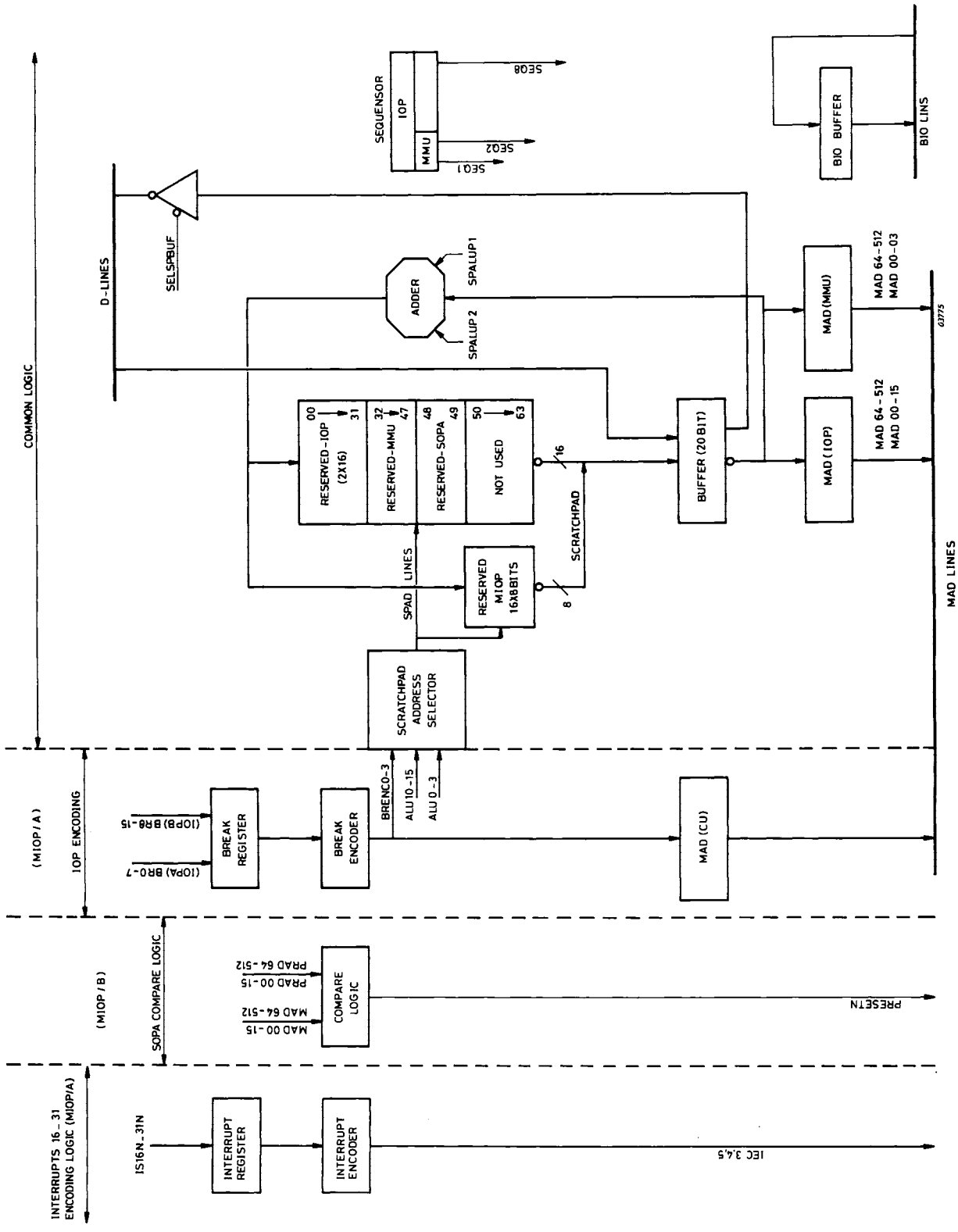


Figure 3.15A MIOP ARCHITECTURE

3.15.1 COMMON LOGIC (FIGURE 3.15B)

The Common Logic comprises the MIOP Scratch-Pad with its associated Addressing and Buffer Logic and the MIOP Sequensor, see Figure 3.15B.

MIOP SCRATCH-PAD ADDRESSING

The MIOP Scratch-Pad is addressed via SPAD 00-05 lines which contain a Scratch-Pad address 0-49. There are 3 modes of operation selected by signals BRENCAD and BSYCPUEXN (see Table inset in Figure 3.15B); these are:

- MMU Mode, here the MADMMU lines are selected which contain the address of the Segment Table sent from the CPU via MADS00-03.
- IOP Mode, here a code from the Break Request lines addresses one of two control words. A third control word is addressed together with the second one.
- Load Scratch-Pad Mode, here the ALU lines are selected to load either the
- Control Words of the IOP, the Segment Table of the MMU or a Preset Address for SOPA.

MIOP SCRATCH-PAD BUFFER LOGIC

The Scratch-Pad Buffer (SPBUF) is a latch (type LS398) which inverts the data that appears at its inputs, after this Buffer the data path depends on the function IOP, MMU or SOPA. This Buffer also receives an input from the Bus D from the CPU for Load Scratch-Pad operations (SELR2=1).

MIOP SCRATCH-PAD LOADING

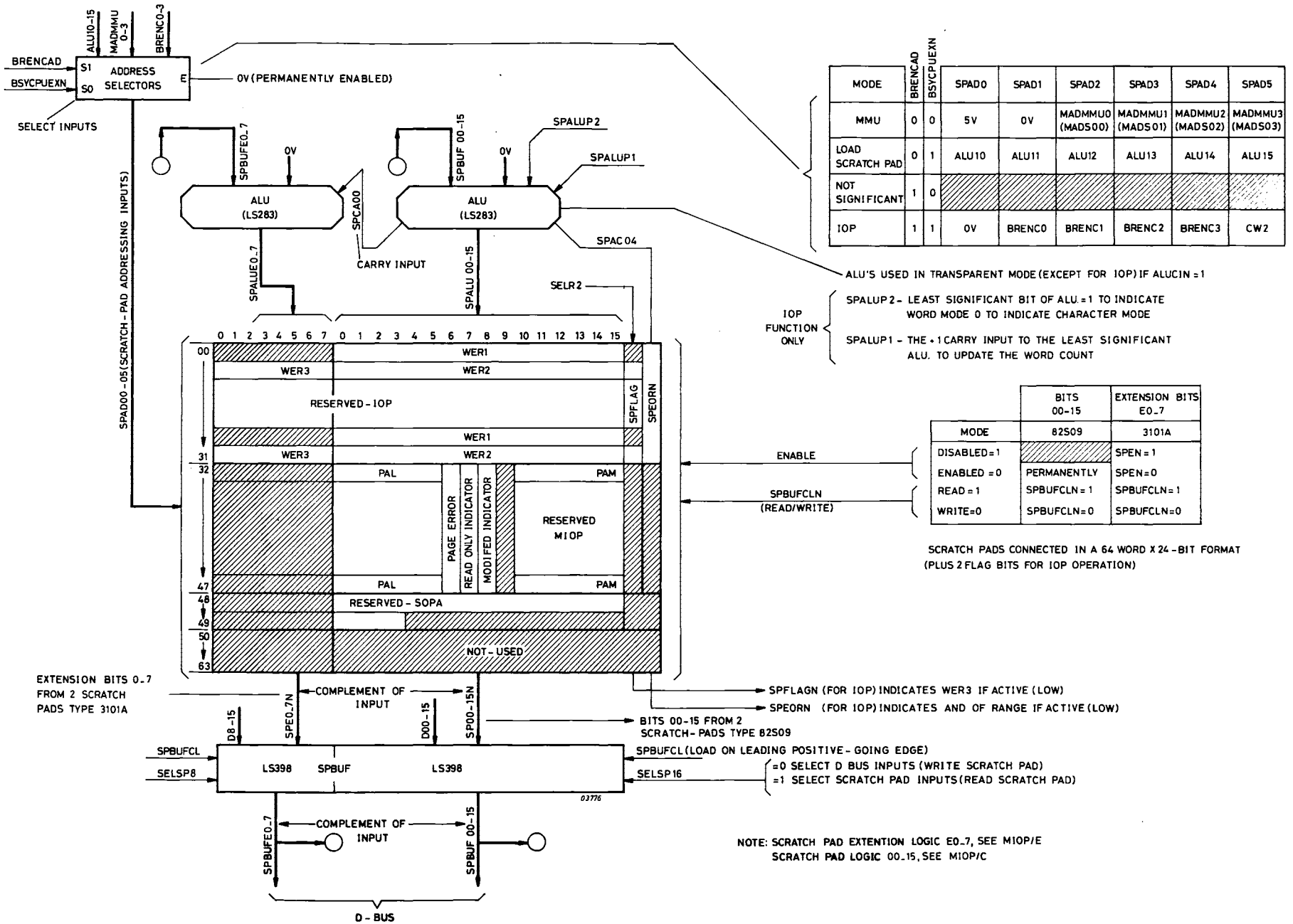
At the Scratch-Pad data inputs an ALU function receives the SPBUF lines which are then written onto SPALU 00-15 in true value to load the Scratch-Pad at a selected address. For MMU and SOPA Functions the ALUs are used in Transparent Mode and it is only for IOP operation that the other inputs SPALUP2 (word or character operation) and SPALUP1 (update word count) are used.

MIOP SCRATCH-PAD

The MIOP Scratch-Pad has a 64 word x 24-bit format but as can be seen from Figure 3.15B the shaded areas are not used. The MIOP Scratch-Pad uses 4 components; 2 x 82S09 (bits 00-15 + 2 Flag bits for IOP) and 2 x 3101A (extension bits E0-E7). For IOP 3 Control Words are contained at 2 addresses for each Break Level. For MMU the Segment Table is written in a 16-bit x 16 word format. The reason for writing the Preset Address into the Scratch-Pad (SOPA) is to facilitate the reading back of the Preset Address with Control Panel Key (RPA).

MIOP SEQUENSOR

The MIOP Sequensor is primarily used to control the sequence of IOP transfers and the IOP Function uses the Sequensor from Count 1 to Count 8. The MMU does use the Sequensor from Count 1 up to Count 2 which serves as a delay during the MMU Translate cycle but at Count 3 the Sequensor is blocked. A summary of Sequensor operations is given in Table 3.16.



MODE	BRENCAD	BSYCPUEXN	SPAD0	SPAD1	SPAD2	SPAD3	SPAD4	SPAD5
MMU	0	0	5V	0V	MADMMU0 (MADS00)	MADMMU1 (MADS01)	MADMMU2 (MADS02)	MADMMU3 (MADS03)
LOAD SCRATCH PAD	0	1	ALU10	ALU11	ALU12	ALU13	ALU14	ALU15
NOT SIGNIFICANT	1	0						
IOP	1	1	0V	BRENC0	BRENC1	BRENC2	BRENC3	CW2

ALU'S USED IN TRANSPARENT MODE (EXCEPT FOR IOP) IF ALUCIN = 1

IOP FUNCTION ONLY

SPALUP2 - LEAST SIGNIFICANT BIT OF ALU. = 1 TO INDICATE WORD MODE 0 TO INDICATE CHARACTER MODE

SPALUP1 - THE + 1 CARRY INPUT TO THE LEAST SIGNIFICANT ALU. TO UPDATE THE WORD COUNT

MODE	BITS 00-15 82S09	EXTENSION BITS E0_7 3101A
DISABLED = 1		SPEN = 1
ENABLED = 0	PERMANENTLY	SPEN = 0
READ = 1	SPBUFCLN = 1	SPBUFCLN = 1
WRITE = 0	SPBUFCLN = 0	SPBUFCLN = 0

SCRATCH PADS CONNECTED IN A 64 WORD X 24-BIT FORMAT (PLUS 2 FLAG BITS FOR IOP OPERATION)

Figure 3.15B COMMON LOGIC - SCRATCH PAD ADDRESSING

Input Signal	Pin	Output Signal	Pin	Summary of Sequensor operation (see CP7R/A) IOP	MMU
SEQ1D	3	SEQ1	2	After a Break Request is decoded (BRENCADN=0) and if the CPU is not busy with the Bus the Sequensor is started in anticipation (SEQ1D = 1).	The Sequensor is started (SEQ1D=1) when the CPU indicates that a Translate cycle is required (BSYEXDLN=0) and the IOP is not Busy with the Bus.
SEQ1	4	SEQ2	5	SEQ1 enables SEQ2 at the next OSC90A	SEQ1 enables SEQ2 at the next OSC90A clock. SEQ2 enables the Scratch-Pad to be written. Only the M bit (Modified) can be written (SELSP16=1). The sequensor stops here.
SEQ3D	7	SEQ3	6	SEQ2. BRENCAD enables SEQ2IOP to set SEQ3D high enabling SEQ3 at the next OSC90A clock. Note that SEQ3 must wait here until IOP is ready.	This is the end of the Translate cycle so SEQ3D is blocked by BSYCPUNB=0.
SEQ4D	8	SEQ4	9	Here the Sequensor must Wait until the Bus is given to the IOP. OSC90A from the CPU synchronises BSYIOP enabling BSYIOPSN to enable SEQ4D. Before the SEQ5 Count is enabled the first exchange takes place (OTR or INR).	
SEQ5D	13	SEQ5	12	TSMIOP enables SEQ5D. The sequensor waits here until the	
SEQ5	14	SEQ6	15	first of the two exchanges is finished. Also the BIO buffer is clocked and Timing Master to Slave is reset (TMRN or TMPN).	
SEQ6	17	SEQ7	16)	Second Exchange is started and the content of the BIO	
SEQ7	18	SEQ8	19)	buffer is enabled to the BUS, controlled by SELMEM, TSM2. MSN is reset and when this exchange is finished, also BSYIOP is reset. During the CU-IOP exchange the Control Unit will reset its BREAK request.	

Table 3.16 MIOP SEQUENSOR

3.16 IOP OPERATION (FIGURE 3.16)

The principles of IOP operation are given in par. 3.16.2. The operation may be considered in four parts:

- Prepare the Exchange (WER)
- Control Unit sends Break
- IOP requests the Bus
- Exchange.

3.16.1 PREPARE THE EXCHANGE

To prepare for the exchange the parameters must be loaded into the Scratch-Pad with instruction WER1, WER2 and WER3. The loading of these instructions is under Microprogram control (see Figure 3.16A) and the data path is shown in Figure 3.15B and 3.18A.

WER1

WER1 contains the parameters: length, character or word operation, input or output exchange and the bits MADE6, MADE7, (see chapter 2.4.2). Bit 15 of the WER is tested and if "0" the Microprogram executes the WER1 part of the routine. SPFLAG is reset to 0 and word 1 is loaded. The Scratch Pad Extension (SPE) is loaded with address bits MADE6, 7.

WER2

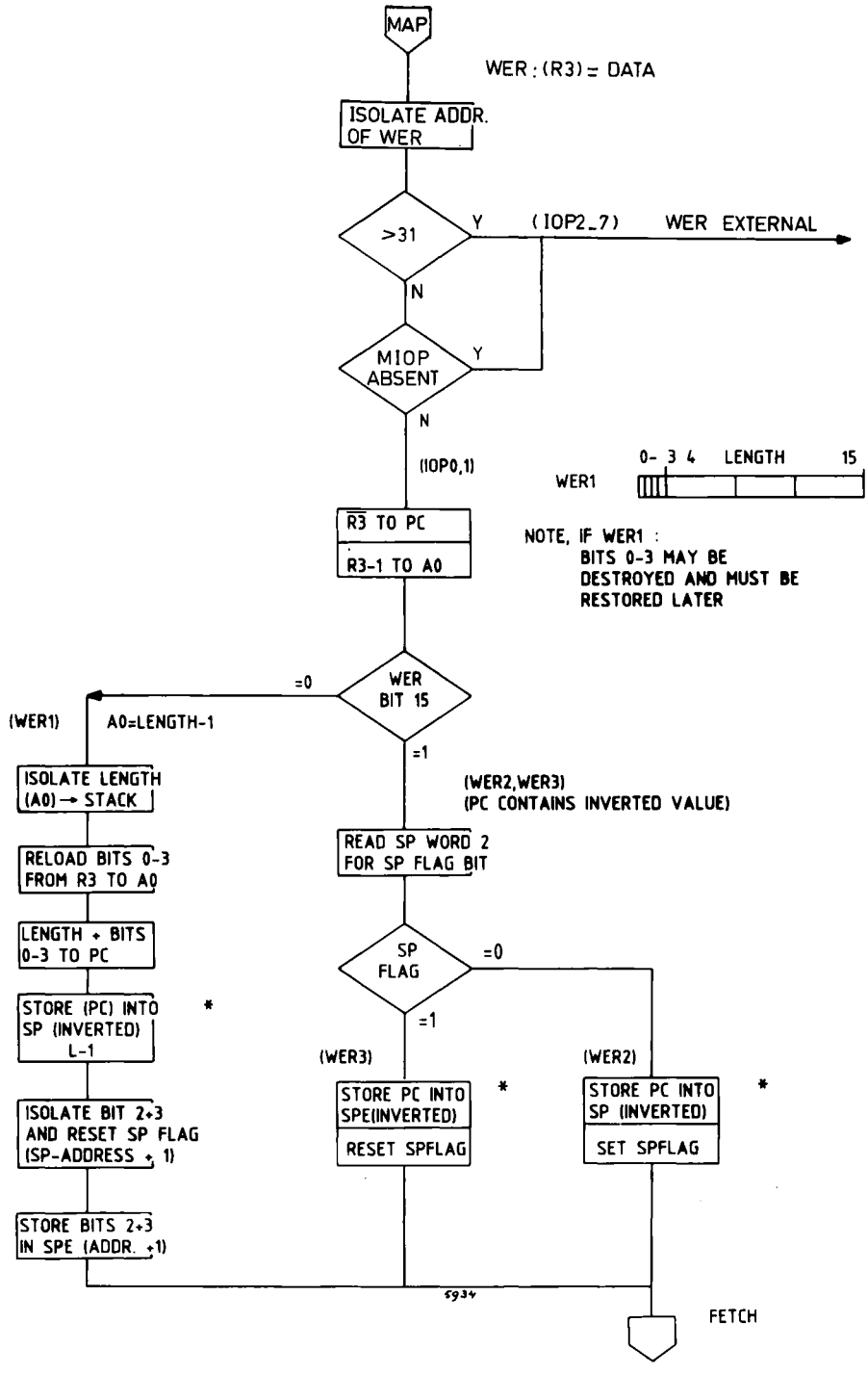
WER2 contains, the address. Bit 15 of the WER is tested and if "1" the microprogram goes to the WER2/3 part of the Routine. As this is the WER2, (SPFLAG = 0, here the address is loaded into the Scratch-Pad and the SPFLAG is set to "1" (the address is loaded via the D lines). If no WER3 is programmed then the content of the Scratch-Pad remains as it is now.

WER3

Here Bit 15 is tested (=1) and then SPFLAG is tested (=1) so the Microprogram loads the most significant bits of the address from the D lines into the Scratch-Pad Extension (types 3101A). First CW2 is read so that the value of SPFLAG is known and then loaded back into the same address in Scratch-Pad. SPFLAGN is written onto FLAGCW3N in true value and FLAGCW3N (MIOP/E) is a test input for the CPU Microprogram Controller. In this way the Microprogram recognises either a WER2 or WER3 routine. At this point the MIOP Scratch-Pad contains the exchange parameters and so the exchange may now be started.
The previously loaded bits MADE6 and MADE7 are overwritten in the Scratch-Pad Extension.

3.16.2 IOP OPERATION

The CPU is responsible for the initiation of the C.U. with a CIO Start. This CIO switches the C.U. from Inactvie to the Exchange state (for OTR) or to Execute (for an INR). For purposes of this example consider an CIO Start Output is executed so that the C.U. switches to Exchange and raises a request (for this example BR1ON, see MIOP/A). Once the Break is active the MIOP requests the Bus and starts the IOP Sequensor. This Sequensor is responsible for the control of the Exchange.



* NOTE: VALUE LOADED IN SP OR SPE IS INVERTED
IN THE SCRATCHPADD BUFFER DURING LOAD OPERATION (D→SPBUF)
ALSO THE LENGTH IS DECREMENTED BY ONE AGAIN AT THE SAME TIME

Figure 3.16A IOP MICROPROGRAM - PRINCIPLE OF OPERATION

3.16.3 CONTROL UNIT SENDS BREAK

The Break Control Logic receives the Break Requests from the Control Units in two groups. IOPA (BR00N-BR07N) and IOPB (BR08N-15N) are latched in F/Fs type LS373 and then encoded in encoders type LS348. If a Break occurs in the group IOPA then signal BREN inhibits the encoding of IOPB. For this example consider that there is a Break BR10N. In this case the outputs are as follows:

- BRENC0 = 1 (input to the OK0A logic)
- BRGS1N = 0 (input to the OK0B logic)
- BRENC0-3 (4-bit code representing the BR10N level)
- BUSRQE = 1 (input to the Bus Request logic).

At this point an exchange is requested so the responsibility to continue is with the IOP Bus Request Logic.

3.16.4 IOP REQUESTS THE BUS (MIOP/F, MIOP/G)

The Bus Request Logic is already explained in par. 3.10. At the same time that the Bus Request is made (BUSRN) the IOP Sequensor is started (BRENCADN).

3.16.5 EXCHANGE CONTROL

The exchange is under control of the MIOP Sequensor. A summary of the events is given in Table 3.16 and the timing for the INRs and OTRs in Figures 3.16B and C. For purposes of this description operation is described as follows:

- Start Sequensor
- Execute OTR or INR

START SEQUENSOR (CP7R/A)

The Sequensor is started in anticipation of the Bus being given to the IOP. Then BRENCADN may initiate the IOP Sequensor cycle. The Sequensor counts up to SEQ3 and waits here for the IOP to take the Bus. When the IOP has the Bus the Sequensor is incremented to SEQ4.

EXECUTE OTR OR INR (Figures 3.16B and C)

The operation of the Sequensor now depends on whether an OTR or INR is to be executed. Two exchanges must be controlled which differ for OTR or INR.
INR - CU to IOP and IOP to MEMORY
OTR - MEMORY to IOP and IOP to CU.

Bit 01 of Control Word 1 is used to control a multiplexer LS157 (MIOP/F) via signal WRIOP. In this way the correct order of the exchanges is followed during the sequensor operation.

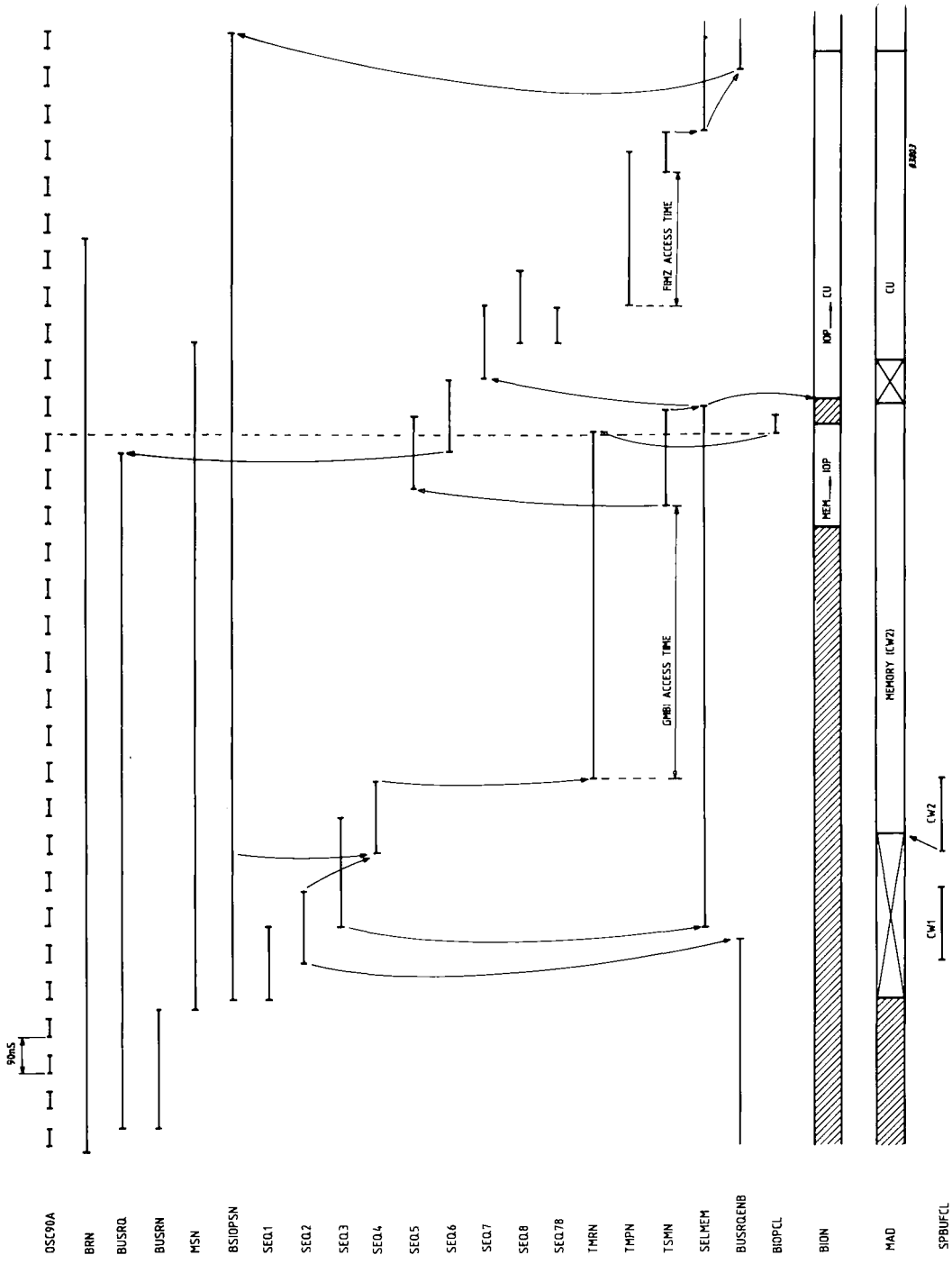


Figure 3.16B MEMORY TO CU (OTR)

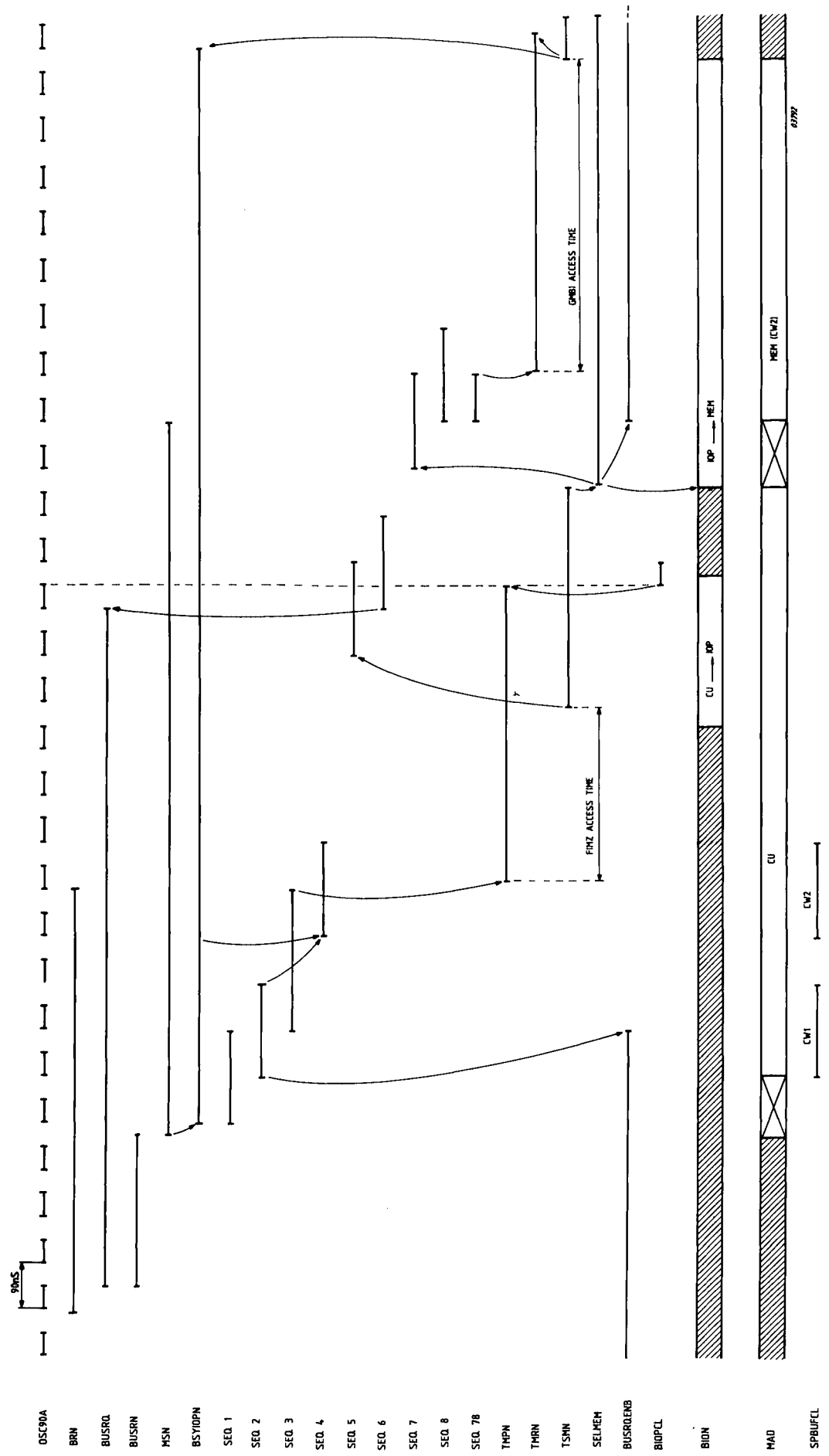


Figure 3.16C CU TO MEMORY (INR)

3.17 MEMORY MANAGEMENT UNIT (FIGURE 3.17)

The Memory Management Unit (MMU) enables the P857E to address up to 8M words by extending the addressing capability to 24 bits. The principle of operation and formats is given in Chapter II. For purposes of this description the MMU Function is described in 5 parts:

- Loading Segment Table
- Translation Cycle
- Modified Page
- Page Fault Detection
- Successful Memory Access

3.17.1 LOADING SEGMENT TABLE (FIGURE 3.17A)

The loading of a Segment Table is achieved with instruction TL which is executed in System Mode. The Segment Table comprises 16 words which are loaded under the control of the CPU Micro-Program (see Figure 3.17A) into the MMU Scratch-Pad. At this point the MMU Function is loaded and ready to be used when the CPU changes to User Mode.

3.17.2 TRANSLATION CYCLE (FIGURE 3.17B)

The start of a Translation cycle is indicated by signal BSYCPUEXN = 0 from the CPU and the end of this cycle is indicated by signal OKMMU = 1 from the MMU. For purposes of this description the Translation Cycle is described in 3 parts:

- CPU loads MADS
- MMU reads the Scratch-Pad
- Address Memory

At this point the Segment Table was already loaded into the Scratch-Pad.

CPU LOADS MADS

The system is in User Mode and an address is loaded from CPU (via MADS00-03) to the MMU. This address (MADS00-03) is written onto the MADMMU lines and then onto SPAD0-5 to address one of the 16 words in the MMU Table.

MMU READS THE SCRATCH-PAD

The MIOP Sequensor is started BSYEXDLN = 0 and the Scratch-Pad is addressed (via SPAD0-5). The MIOP Sequensor counts up to SEQ2 and is then inhibited by signal BRENCAD = 0. Before SEQ2 time the Scratch-Pad is read and the content written already onto the MAD00-03, MADE 0 to 7 lines.
The Scratch pad is rewritten during SEQ2 (SPCLN = 0).

ADDRESS MEMORY

The MMU has written a 12-bit value (PAL and PAM) onto the MAD lines. At the beginning of BSYEXDLN = 0 signal OKMMU started the sequence to generate TMRN. CPU has the Bus and signal BSYCPUN = 0 enables the CPU to write a 12-bit value (displacement) onto the MAD lines.

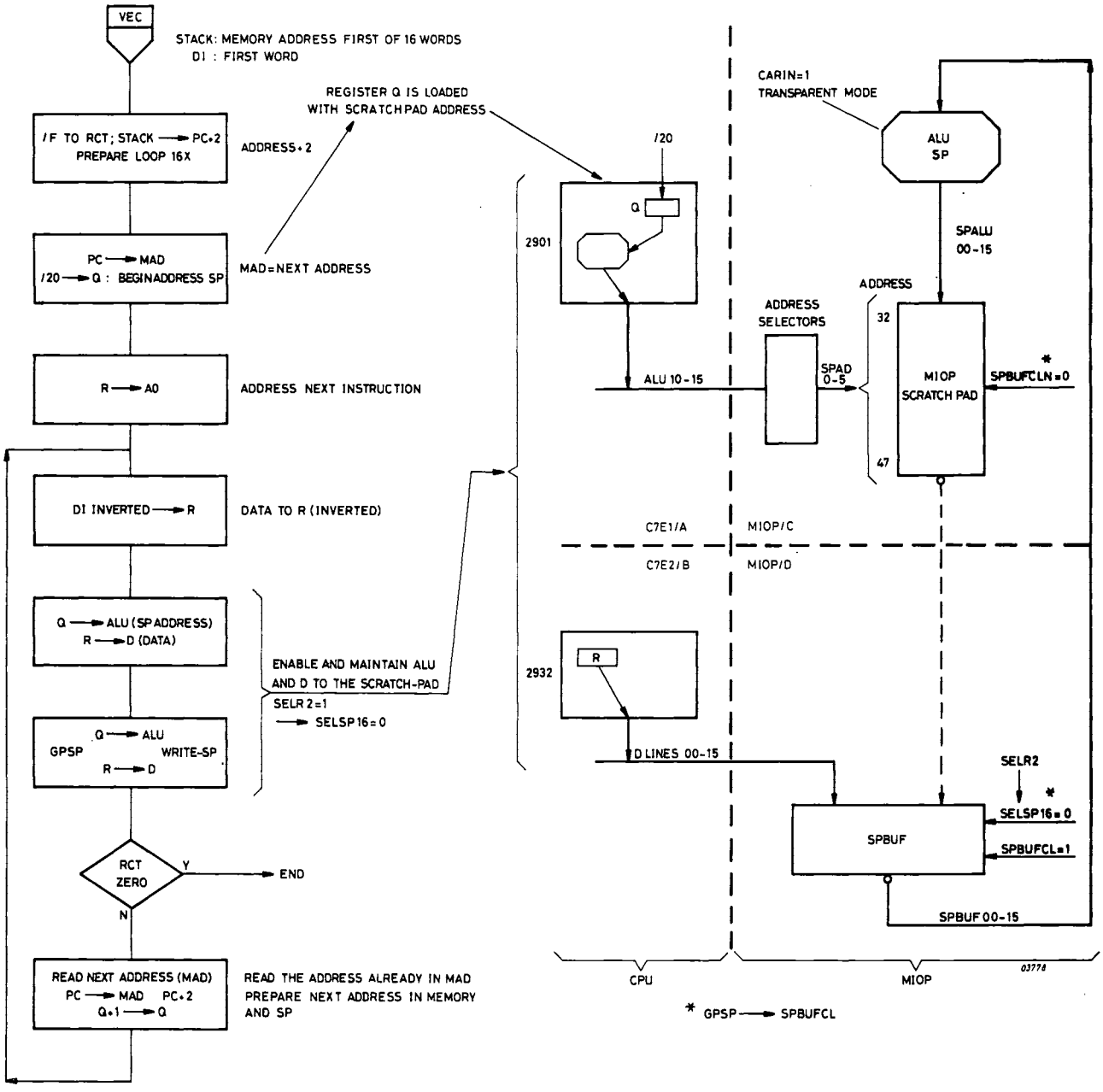


Figure 3.17A MMU - LOAD SEGMENT TABLE

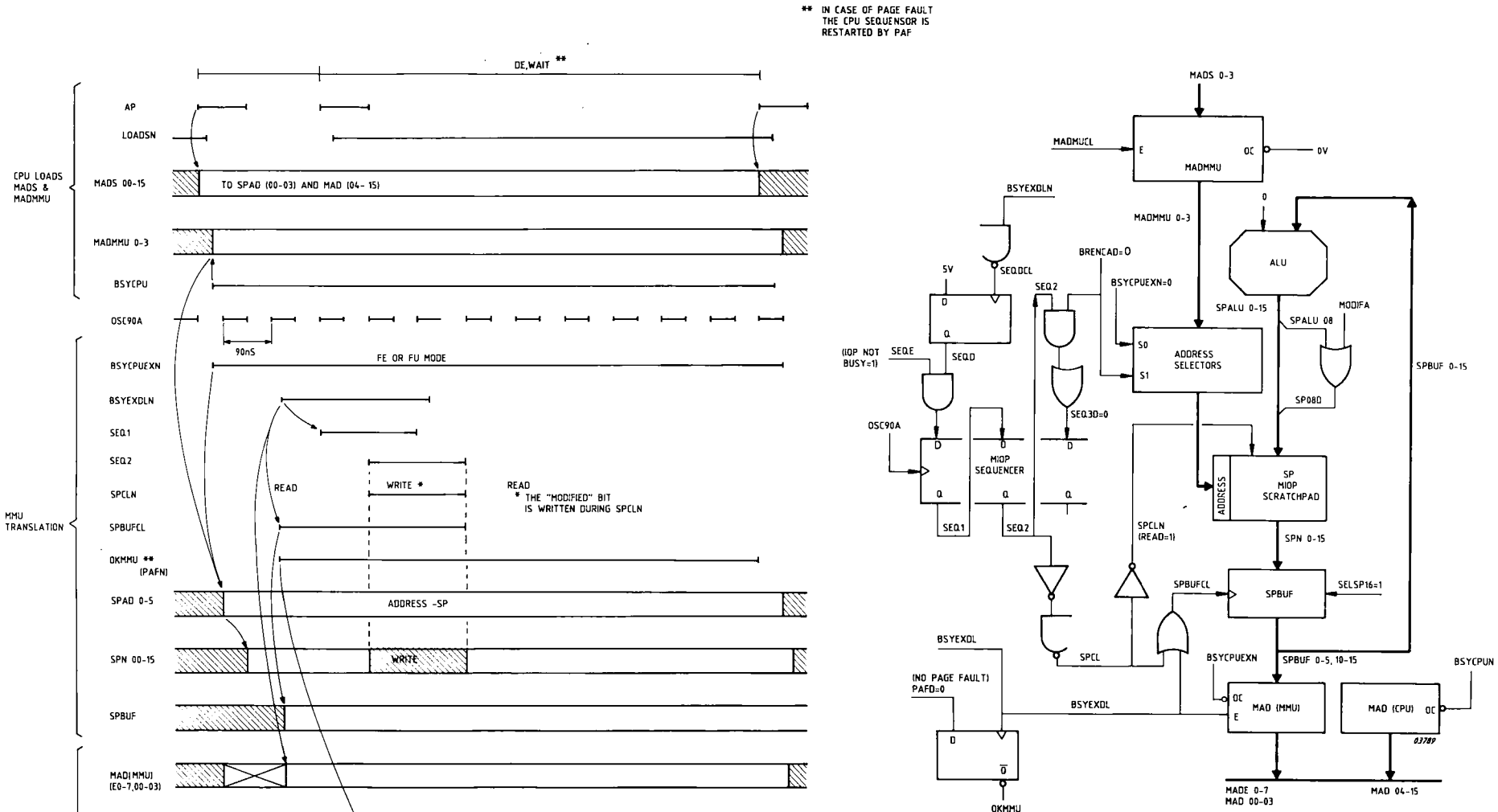


Figure 3.17B MMU - TRANSLATION CYCLE

3.17.3 MODIFIED PAGE (MIOP/C, MIOP/G)

When a page is modified signal MODIFA writes into bit SP08. During the translation request BSYCPUEXN = 0 and signal WRITE = 1 (WRITEMN = 0) so if there is no Page Fault (PAFT = 0) then the modified bit is set in that page.
This is done during SEQ2 when the content of SPBUF is written into the scratch pad (SPCLN=0).

3.17.4 PAGE FAULT DETECTION

A page fault occurs when the program tries to access a protected page. A page fault may occur when any of the following conditions exist (system in Usermode FUN = 0):

- A Write operation is attempted on a Read Only Page (SP07N = 0 ored with WRITEMN = 0).
- The access of a Protected Page (SP06N = 0).

If any of these conditions exist, then at time SEQ2 and BSYEXDL the Page Fault F/Fs activate the PAFN and PAFTN signals which have the following functions:

- PAFTN indicates to the CPU Micro-Program Sequensor (2910) that a page fault has occured and the CPU executes the PAF Micro-Routine.
- PAFN indicates to the CPU Sequensor that an attempt has been made to access the memory, as this access was unsuccessful. PAFN restarts the CPU Sequensor which is in a WAIT cycle.

3.17.5 SUCCESSFUL MEMORY ACCESS

When the memory is accessed and there is no page fault (PAFD = 0) signal OKMMU is enabled to indicate to the CPU that the MIOP has loaded the MAD Register. OKMMU starts the process of sending the TMRN signal. A delay of 180nS is introduced and so the delayed BSYDL signal ensures that the MAD lines are stable before enabling TMRN. OKMMUN stays active until it is reset by the signal PAFZON =0.

3.18 STOP ON PRESET ADDRESS (FIGURE 3.18)

The principal of the Stop On Preset Address (SOPA) function is already described in Chapter II. For purposes of this description SOPA operation is described in 4 parts:

- Load PRAD and Sratch-Pad
- Reset Preset Address
- Compare Operation
- Read Preset Address

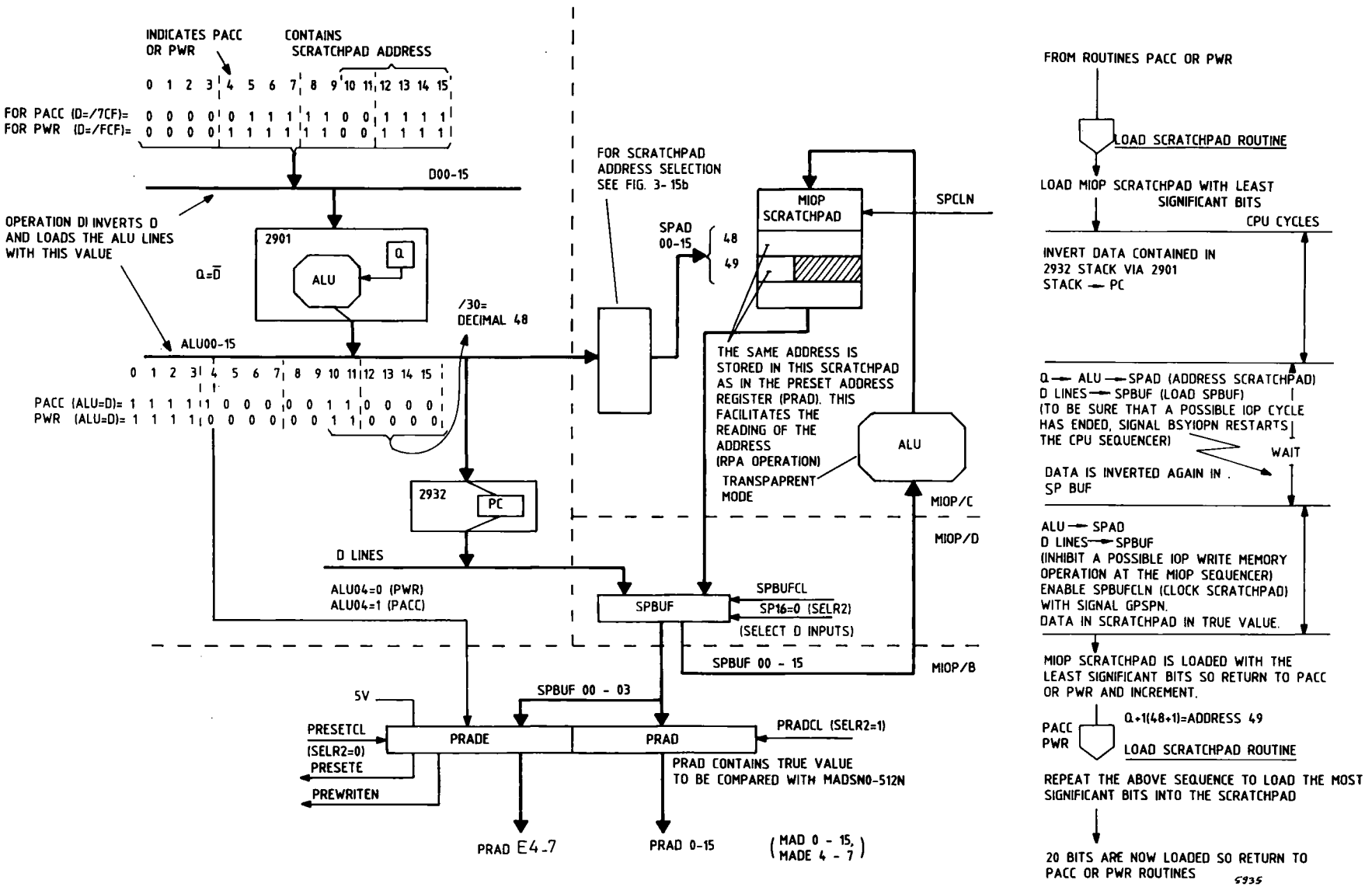


Figure 3.18A LOAD SCRATCHPAD AND PRAD - PACC OR PWR

3.18.1 LOAD PRAD AND SCRATCH-PAD (FIGURE 3.18A)

The Preset Address is loaded for either Preset Access-Read and Write (PACC Micro-Routine) or for Preset Access-Write Only (PWR Micro-routine). The only significant difference between these routines is in the value of ALU04 which is used to indicate PACC or PWR. The Scratch-Pad address of decimal 48 is a constant from the Micro-Program NAD lines. The Load Scratch-Pad Routine is responsible for the loading of the Scratch-Pad Buffer (SPBUF) and then the simultaneous loading of the Scratch-Pad and PRAD. Two words are loaded; the 15 least significant bits into address 48 and the 4 most significant bits into address 49. The data paths and significant signals are shown in Figure 3.18A).

The Preset Address was stored in the 2932 stack during the microprogram routine PUP. Before loading into the Scratch-Pad can be executed the value from the 2932 stack is routed via the 2901 and inverted, stored in PC (2932) and routed to the D-bus again. The scratch pad is addressed via ALU-bus from register Q (2901).

3.18.2 RESET PRESET ADDRESS

This is a Micro-Routine comprising one Micro-instruction called POFF (Preset OFF). When the Preset Off function is selected at the Control Panel the POFF Routine enables signal GPRESETN = 0 to activate signal PRADZON (when WRITEMN - APMN) conditions exist). PRADZON resets the PRAD Register to 0 (see Figure MIOP/B). In this way also PRESETE is reset to disable the compare logic.

3.18.3 COMPARE OPERATION (FIGURE 3.18B)

The PRAD and Scratch-Pad are loaded with a Preset Address and when one of the 3 conditions take place signal PREVAL = 1 to enable a comparison to be made between the PRAD and MAD lines. These 3 conditions are:

- Memory Access-Read and Write (Memory Write)
- Memory Access-Read and Write (Memory Read)
- Preset Write Only (Memory Write)

Signal PREVAL = 0 to inhibit a comparison between the PRAD and MAD lines when one of 2 conditions exist. These 2 conditions are:

- PRESETE = 0 indicates that there is not a Preset Address loaded into the PRAD Register.
- Preset Write Only (Memory Read)

The PREVAL Truth Table in Figure 3.18B shows the logic levels of these 5 conditions.

3.18.4 READ PRESET ADDRESS (FIGURE 3.18C)

The Function Read Preset Address (RPA) is controlled by a Micro-Routine of the same name. The responsibility of this routine is to address the Scratch-Pad and read the content into SPBUF and then assemble the 20 bits into 2901 Registers A0 and Q. Once the 20 bits are ready routine SENDADR is responsible for sending this address to the Control Panel. The data paths and significant signals are shown in Figure 3.18C.

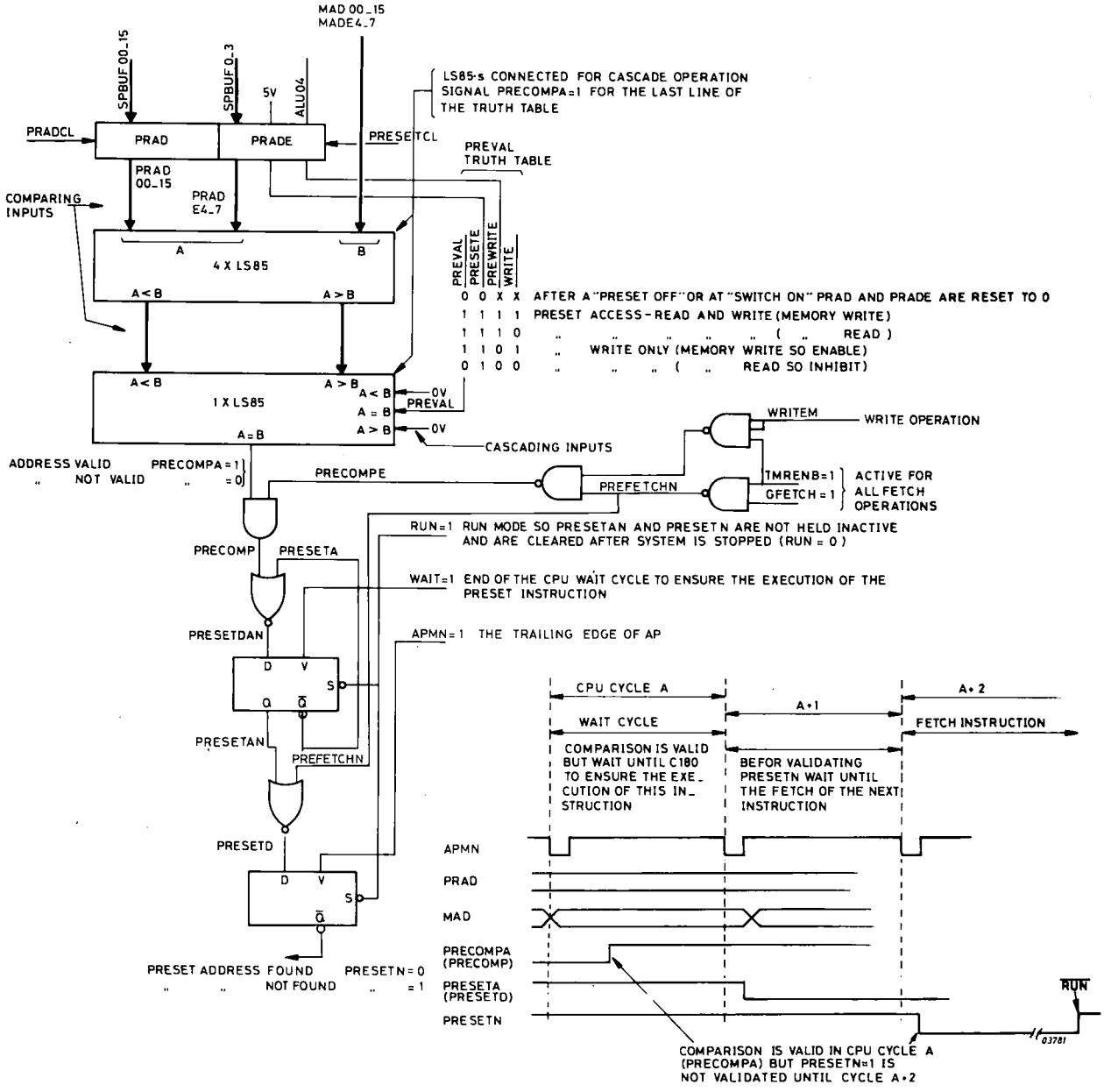


Figure 3.18B SOPA - COMPARE OPERATION

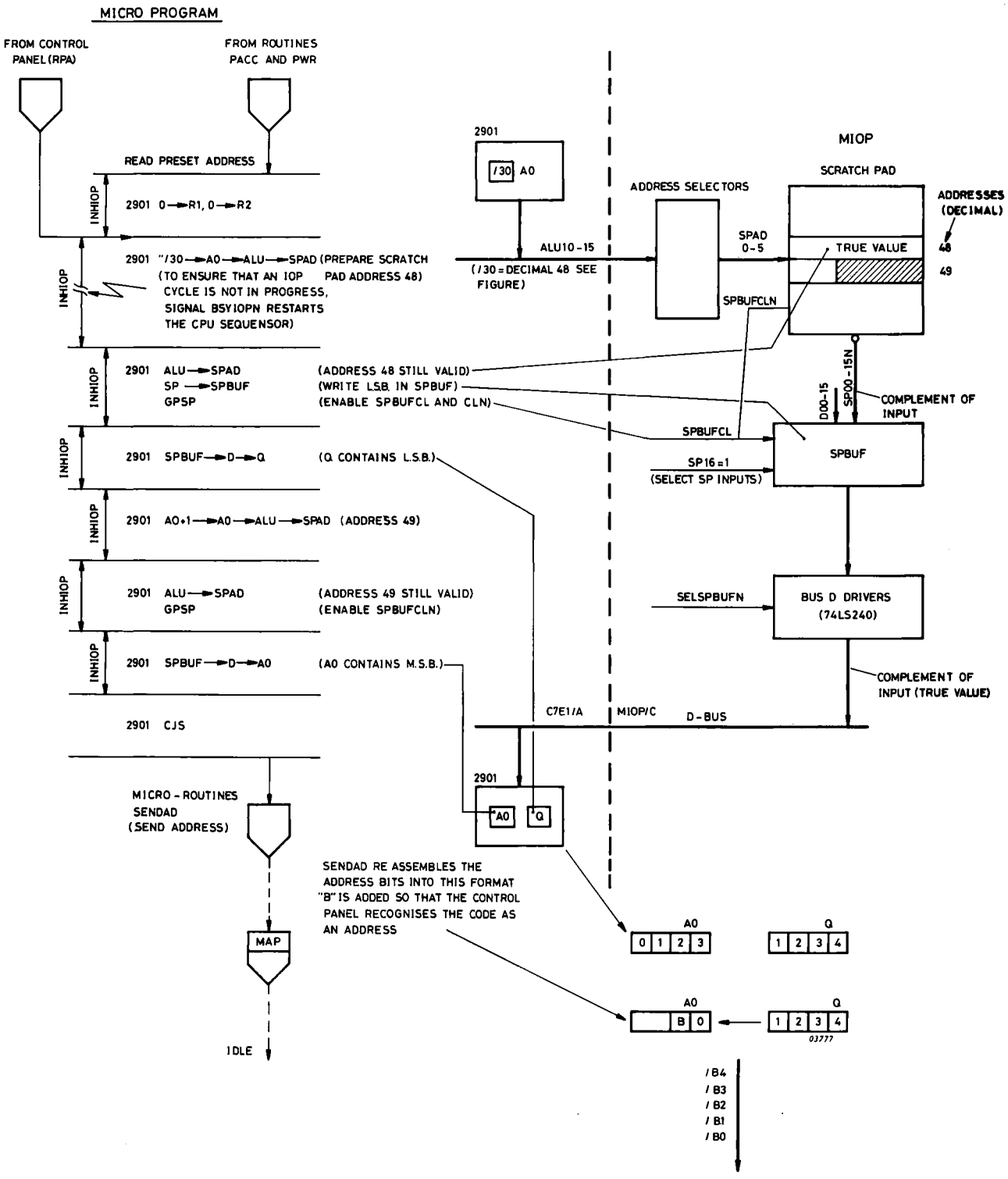


Figure 3.18C SOPA - READ PRESET ADDRESS

3.19 MICROROUTINES DESCRIPTION

This section describes in detail some parts of the microprogram routines and subroutines. This should enable the user to follow other microprogram sequences using only the microprogram flow charts.

3.19.1 ROUTINE DESCRIPTIONS

INITIATE P857 SYSTEM

At switch-on the Microprogram Counter (MPC) is reset to /000 which is the address from which the Initiate sequence begins. This is done by the instruction JZ which was forced on the ROMF bits: 10, 11, 12, 13 (ROMADI 0 - 3).

ROUTINE RSL (MICROROUTINE Figure 1b)

Address /000
- 2901 Not significant
- 2932 Reset
- 2910 The microprogram field (MPF) bits 10-13 indicate /3 which is a conditional jump to pipeline (CJP) and so the next microprogram address is taken from NAD bits 44-55 which specify address /687.

Address /687 Load Constant in Reg Q
- 2901 Load Constant in Register Q which has the value /CE and is the Mode Instruction for 8251 (Control Panel). The details of the Mode Instruction are given in par. 3.7. The data path for the constant (/CE) is shown in Figure 3.3D/A. The Select D Field is /001 enabling signal SELCONSTN to allow the input of the emitters onto the D Bus. Register Q is loaded via ALU path so port R directly receives the first operand (content of D) and for the second operand S=0. The ALU result is R+S which in this example is /CE. The destination field of ALU is /000 (I6, I7, I8) specifying a Load Q (LDQ) so ALU writes into Q the value /CE.
- 2932 Operation is not significant. MPF Bits 17-20 indicate Fetch PC+ci. MPF Bit 21 PCCIO=0 indicates ci=0 therefore PC+0=0. In this case we have the equivalent of a NO Operation (NOP).
- 2910 MPF Bits 10-13, indicate a Continue (/E) operation. The MPC executes PC+1 to PC so in this case the next address is /687+1=/688.

Address /688 Load a constant into RCT
- 2901 Not significant
- 2932 Not significant (PCI=4, PCCI=0)
- 2910 The RCT is going to be loaded with a count of 16. This value serves as a delay to respect the sending of the Mode and Command Instructions to the 8251. The loading of RCT is by an LDCT (/C) operation. A CONT operation increments the PC to /688+1=/689.

Address /689 Call Subroutine Send Command (Figure 3.3D/B)
- 2901 Not significant
- 2932 Not significant
- 2910 A Jump to Subroutine (CJS) Micro-inst is executed which causes a return address /68A to be saved in the Stack and a Branch Address is read from the NAD Field into the MPC. The MPC now contains /518 which is the next address.

SEND COMMAND

The microprogram has now left the routine RSL to perform a subroutine called Send Command. The purpose of this subroutine is to write the Mode Command to the 8251 (Control Panel).

Address /518
- 2901 Not significant
- 2932 Not significant
- 2910 The NAD Field gives the next Address /OFE and 6 of these lines are also used as dedicated control lines as follows:
  - NAD 10 = 1 CDN
  - NAD 09 = 1 WRN
  - NAD 08 = 1 direction ALU/DT lines
  - NAD 06 = 1 inhibit 8251 V24.
  - NAD 05 = 1 enable 2901's
  - NAD 03 = 0 select 8251 Control Panel.

When the NAD Field is read signal CDU goes high to indicate that a Command word is on the data lines. The Micro-inst indicates Cont so PC+1= /519.

Address /519 Load Mode Instruction (Figure 3.3D/C)
- 2932 Not significant
- 2910 Signal CDN is maintained for another 225nS by the constant /OFE and the 8251 (Control Panel) is selected by SELHPN (CS is enabled by SEL8251. NAD03N). A Cont Micro-inst is executed and the MPC incremented by 1 to /51A.
- 2901 Data is transferred from Reg Q to the ALU lines via ALU (ALUI=02).

Address /51A The purpose of these operations is to control the transfer timing signals. Signal WRN is activated by NAD Field /OFA.
- 2932 Not significant
- 2901 Data is maintained on the ALU lines for the 8251
- 2910 The Field NAD contains the function (/OFA) and NAD09 is reset for WRN=0 and CS remains steady. The CPU cycle is 360nS; a Cont Micro-inst is executed to increment the MPC to /51B.

Address /51B To end the Write operation by forcing signal WRN high.
- 2932 Not significant
- 2901 Data is maintained on the ALU lines
- 2910 The NAD Field (/OFE) causes signal NAD09 to go high ending the write operation. The CPU cycle is 225nS; a Cont Micro-inst increments the MPC to /51C.

Address /51C Remove data from the ALU lines and disable the 8251.
- 2932 Not significant
- 2901 Data is no longer maintained
- 2910 Signal SEL8251 is inactive disabling the 8251 (Control Panel). CPU cycle is 225nS; a Cont Micro-inst increments the MPC to /51D.

Address /51D To introduce a delay of 17 x 360n8=6.8 micro seconds into the subroutine.
- 2932 Not significant
- 2901 Not significant
- 2910 Between the sending of the Mode and Command instructions a delay must be introduced. This delay is achieved with Micro-inst RPCT (Repeat Counter). A value from the NAD lines (in this case 16) is loaded into the Counter at address /688. The execution of RPCT causes 16 + 1 = 17 CPU cycles each with a duration of 360nS to be executed, giving the delay of 6.8uS. A Cont increments the MPC to /51E.

Address /51E To enable a return to routine RSL
2932 Not significant
2901 Not significant
2910 At address /689 the return address /68A was saved in the Stack. Micro-inst CRTN is executed which pops the stack enabling a return to the RSL routine.

Address /68A To call a subroutine CLEAR.
2932 Not significant
2901 Not significant
2910 A CJS is executed which causes a return address /68B/CDd to be saved in the Stack. A Branch Address is read from the NAD Field (/678) and loaded into the MPC.

Address /678 Subroutine CLEAR to enable signal CLEARN (Figure 3.7C/D).
Signal GPBITH enables the CPU to take the Bus for consecutive cycles by setting the BSYH flip flop so that no other Masters may take the Bus before the generation of signal CLEARN.
BSYN is set during the BUS request in the next word /6E4 and held by BSYH.
2901 Not significant
2932 Not significant
2910 Micro-inst CJP takes the MPC to /6E3

Address /6E3 Prepare Command for 8251 (Control Panel).
2932 Micro-inst PSHP protects PC in the Stack otherwise it is lost in the operations that follow. PC is restored at address /6E8.
2901 The constant /005 is loaded into Reg Q; as this is the Command that will be sent to the 8251 in the next Send Command Routine. Microprogram Bits 24 and 25 have the value 11 specifying a LDRM (Load R1). Signal SELCONST enables the value 0 to be loaded from NAD 01, 02, 03, 04 to D05, 06, 07, 08 (R1 Field). (When the R1 Field has a 0 value this means that Reg A0 is the addressed register.)
2910 Micro-inst Cont increments the MPC to /6E4.

Address /6E4 To request the Bus. This Micro-inst obtains the Bus if the following conditions exist:
Exchange Request is active, DE = 1
No Bus Requests from the System Masters, BUSRN = 1
No Bus allocations are being made, MSN = 1
Bus is free, BSYN = 1, SPYC = 1, TRMN = 1 and TPMN = 1.

At this address the conditions of the exchange are now specified:
TMRENB, Signal TMRENB = 0 inhibits the sending of TMRN
GFETCH, Signal GFETCHN = 0 to set SEQSYN = 0 to resynchronise the Sequensor.
The CPU Sequensor is held in a WAIT cycle until the Sequensor is resynchronised.
2932 Not significant
2901 At address /6E3 Reg A0 was selected and now the value /BF is loaded (see Figure 3.3D/D). This constant is used to initialise the PSW.
2910 Micro-instruction Cont increments the MPC to /6E5.

Address /6E5 Load Counter to enable CLEARN to be maintained for about 90uS.
2932 Not significant
2901 Not significant
2910 Execute Micro-instruction RCTLD to load the constant /F0. This constant acts as a delay at the end of the subroutine Send Command to maintain the signal CLEARN low for a duration of 90uS. Micro-instruction Cont increments the MPC to /6E6.

Address /6E6 To initialise the PSW and call the subroutine Send Command (Figure 3.3D/E)

2932 Not significant

2901 Initialise the PSW by activating the commands SELPSWN and ALUCIN. The CPU is in Enable Interrupt Mode and Bit FU=0. Signal ALUCIN resets signal PWF = 0 (Note that the bits in PSW8-15 are inverted).

2910 In order to send the Command word (already loaded in Q at address /6E3) to the 8251 Control Panel the Send Command subroutine is called. A CJS is executed which causes a return address /6E7 to be saved in the Stack and a Branch Address is read from the NAD Field into the MPC. The MPC now contains /518 which is the start address of the subroutine Send Command.

SEND COMMAND

This subroutine is already described previously. The purpose of this paritcular Send Command is to reset the DTR F/F in the 8251 to set CLEARN low. CLEARN is set high during the next Send Command Routine.

Address /518 Generate NAD Control Lines
Address /519 Load Command Instruction
Address /51A Write Operation.
Address /51B End Write Operation
Address /51C Remove Data and Disable 8251
Address /51D To introduce a delay into the subroutine
Address /51E To enable a return to routine CLEAR

2910 At address /6E6 the return address /6E7 was saved in the Stack. Micro Instruction CRTN pops the Stack enabling a return to the CLEAR routine.

Address /6E7 Load MAD Extension Lines wih zeroes. Prepare Command Q = /0007.
Address /6E8 Restore P and load constant into RCT

2932 Execute Micro-inst RTS to recover P which was stored in the stack at address /6E3.

2901 Not significant

2910 In preparation for the Send Command routine the constant /10 is loaded into the RCT by executing Micro-inst LDCT (Load Counter). Micro-inst Cont increments the MPC to address /6E9.

Address /6E9 Call the Send Command Routine to force CLEARN high and load PLR.

2932 Not significant

2901 The value 63 is loaded into the PLR. Q already contains /0007 and the inverse of this value on the ALU lines 0, 1, 2, 3, 4, 5 = 111111. This change is effected by signal GPLRLD. The CR has a value of /0 for the duration of CLEARN.

2910 In order to send the Command Word (already loaded in Q at address /6E7) to the 8251 (FRCP) the Send Command subroutine is called. A CJS is executed which causes a return address /6EA to be saved in the Stack and a Branch Address (/518) is written by NAD into the MPC. The MPC now contains the start address of Send Command Routine.

SEND COMMAND

This routine is already described. The purpose of this particular Send Command is to set the DTR F/F in the 8251 and set CLEARN high.

Address /518 Generate NAD Control Lines
Address /519 Load Command Instruction
Address /51A Write Operation
Address /51B End Write Operation
Address /51C Remove Data and Disable 8251
Address /51D Introduce a Delay

Address /51E
2910 At address /6E9 the return address /6EA was saved in the Stack. Micro-inst CRTN pops the Stack, enabling a return to the CLEAR routine.

Address /6EA The CPU Sequensor is in a WAIT cycle and an exchange request (DE) is active. This exchange is requested with GPBITH not active so the BSYN signal will be removed after this wait cycle because flip flop BSYH is reset now. The wait cycle is ended by resynchronisation of the sequensor with GFETCH active and TMRINH again.

Address /6EB Load constant /FA into Q

Address /6EC Jump to Routine SCV24 to send the Mode Instruction for the 8251-V24. After the Mode Instruction is sent a return is made to the CLEAR Routine address /6ED (Mode is 2 stop bits, Parity Even, 7 bits factor 16 x).

Address /6ED Zero value for SCV24 command to Q register.
Address /6EE SCV24 to reset the command buffer in the 8251-V24.

After the Command is sent the Interface is now programmed so a return is made to the CLEAR Routine.

Address /6EF The system was cleared, so a return is made to the RSL routine.

Address /68B Load Q with Constant
2901 A constant from the NAD Field "/100" is loaded into Reg Q. R2 field is zero.
2932 Not significant
2910 Micro-inst Cont increments the MPC to /68C.

Address /68C Jump to routine WAIT (0.5ms).
After 0.5ms a RTN is made to the RSL routine.

Address /68D Decrement register Q.
2932 Not significant.
2901 Q register is decremented by one. (Q was loaded with /100 in word /68B). If Q is zero than ALUZERO is true.
2901 If ALUZERO is not true continue with word /68E.
If ALUZERO is true execute the micro instruction CJP to go to the word /681.

Address /68E Jump to /68C.
The WAIT routine will be repeated 256 times.
The total wait loop is thus 256 x 0.5ms = 128 msec.
This routine was necessary as a delay before the read status operation in the routine STAT (Panel - u-Processor can initiate the panel first).
Next address is /681 (MCL routine).

Address /681 Call Subroutines STAT (Status)
  2932 Not sifnificant
  2901 MPB 26 and 27 have the value 00 representing a R2M1 (R2-1) operation resulting in R2 = 15.
  2910 A CJS is executed; the return address /682 is saved in the Stack and a Branch Address is read from the NAD Field into the MPC.

STAT

This subroutine tests whether or not the Control Panel is in LOCK Mode. To enble a subsequent Branch to subroutines Auto Restart, Bootstrap or VISU.

Address /5C3 Initiate 8251 (Control Panel) Control Signals
  2901 Not significant
  2932 Not significant
  2910 The NAD Field (/OFE) specifies the state of the 8251 control signals (see par. 3.11). A Micro-inst Cont increments the MPC to /5C4.

Address /5C4 Select 8251 (Panel) and disable 2901
  2901 Not significant
  2932 Not significant.
  2910 The NAD Field changes from /OFE to /OBE to disable 2901.

Address /5C5 Read Status
  2901 Disabled.
  2910 The NAD Field changes from /OBE to /OB6 causing NAD08 to go low indicating a read operation. The 8251 status appears on the ALU lines.
  2932 Micro-inst PUSHD loads this status word into the Stack.
  ALUX Signal GPCHA is active to load the status into ALUX to enable the status bit at present in ALU08 to be written into D00.

Address /5C6 End of Read Status
  2901 Disabled.
  2932 Not significant
  2910 The NAD Field changes from /OB6 to /OBE causing NAD08 to go high and end the read cycle.

Address /5C7 Return to Routine MCL, 8251 no longer selected.
  2901 The NAD Field changes from /OBE to /OFE (2901 enabled again).
  2932 Not significant
  2910 Micro-inst CRTN is executed to pop the return address (/682) which was saved in the Stack at address /681.

Address /682 LOCK = 1 so go to either Auto Restart or Bootstrap, LOCK = 0 go to /683.

Address /683 Load Q and select register A0.
  2932 Not significant
  2901 The NAD Lines have a value of /000. SELCONST selects this value to the D- bus. Function LDR2 loads /000 into R2 to select A0. Q Reg is loaded with /0000 (source = /0000).
  2910 A Cont increments the MPC to /684.

Address /684 Load A0 and call subroutine SENDAD
  2932 Not significant
  2901 Operation LDRAYF enables a write in A0 via port R2B. Source is /0000 and this is written into A0.
  2910 A CJS is executed; the return address /685 is saved in the Stack and a Branch Address is read from the NAD Field (/618).

Routine SENDAD (Q and A0 are already loaded so, to continue, a start is made at address /618.)

Address /618 Load RCT
- 2901 Not significant
- 2932 Not significant
- 2910 Operation LDCT indicates that the content of the NAD Field (/00B) is to be loaded into the Counter.

Address /619
- 2932 Not significant
- 2901 Operation SRRA (Shift Right A0:2 Port B) indicates that a shift right is made.
- 2910 Operation RPCT enables the Counter to count down to 0 from 11 (/00B). The operation in the 2901 is repeated 12 times in total in this way.

Address /61A Call Routine WAIT
- 2901 Not significant
- 2932 Not significant
- 2910 A CJS is executed; the return address /61B is saved in the Stack and the Branch Address (/6E0) is read from the NAD Field.

ROUTINE WAIT

To ensure that the Panel 8251 is ready this delay is introduced.

Address /61B Prepare the loop to send 5 characters.
- 2901 Not significant
- 2932 Not significant
- 2910 Operation PUSH is specified which loads the NAD Field (/004) into the Counter and pushes the next sequential address into the Stack (/61C).

Address /61C Isolate and recopy 1 tetrad (Figure 3.3D/I)
- 2932 Not significant
- 2901 Operation LDRAYF isolates 1 tetrad in the register A0 and rewrites it into A0 via port R2B. The tetrad (F) is from the NAD Field.
- 2910 Micro-inst Cont increments the MPC to /61D.

Address /61D Load one Character (Figure 3.3D/J)
- 2932 Not significant
- 2901 Operation LDRAYF isolates a second tetrad in the register A0. The second tetrad (/0B0) is from the NAD Field and is added to the first character via port R2B. The result is a character (/BX) in A0.
- 2910 Micro-inst Cont increments the MPC to /61E.

Address /61E Call Routine TSOC
- 2932 Not significant
- 2901 Not significant
- 2910 A CJS is executed; the return address /61F is saved in the Stack and the Branch Address (5B6) is read from the NAD Field.

ROUTINE TSOC

Send one character to Control Panel (In total 5 address characters will be sent)

Address /6D0 to /6D4 Write a character and save Q into 2932 stack.

Address /6D5 Load a Constant into Q to give a delay before reading status, then jump to subroutine WAITST.
2901 Load constant /067 into Q from the NAD Field. This constant specifies th

ROUTINE WAITST

Loop /067 times using CPU cycle 360 + 225nS to give a delay of 60uS.
Address /067 Reduce the value of Register Q by 1 (Q-1) and test for 000. When 000 is true execute a CRTN to the TSOC Routine.
2901 Reduce the value of Q by 1
2910 Test ZERO and if the count is finished execute a CRTN to return to the main routine. If the count is not finished go to address /068.
2932 Not significant

Address /068 Count is not finished so go back to address /067.
2901 Not significant
2932 Not significant
2910 Execute Micro-inst CJP and go to address /067. The value /067 is given by the NAD Field.

RETURN TO ROUTINE TSOC (COUNT FINISHED)

Address /6D6 Load constant 400 into ALUX (to test bit 13 at Address /6DC).
Address /6D7 Enable NAD Control lines
Address /6D8 Read the status
2901 Disabled.
2932 Not significant
2910 The NAD Field constant /0BE activates the 8251 control signals to read the status.

Address /6D9 Load status in the Stack of 2932
2901 Disabled.
2910 The NAD field continues to activate the 8251 control signals.
2932 Execute Micro-inst PSHD to load the status into the Stack.

Address /6DA
2901 Disabled by NAD05 to give the high impedance state.
2932 Not significant
2910 The NAD Field constant /0FE deactivates the 8251 control signals.

Address /6DB Transfer the Status from the 2932 to the 2901.
2932/2901 The 2932 Stack is popped (Micro-inst POPS) and the status is enabled onto the D lines (DE32). Register Q is loaded from the D lines with Micro-inst LDQ.
2910 The NAD Field constant /0FE disables the 8251 control signals, and enables the 2901 (NAD05).

Address /6DC Test status bit 13, Transmitter Empty (TxEmpty)
2932 Not significant
2901/2910 If bit 13 = 0 then a CJP is made to address /6D7. When bit 13 is 1 then ALU output ALUZERO not active, the test is not passed (TESTN not active) and Micro-inst CJP enables the 2910 to continue to /6DD.

Address /6DD Restore Register Q

2932/2901 The 2932 Stack is popped and the Q value written onto the D lines (DE32). The 2901 Register Q is loaded from the D lines with Micro-inst LDQ. Q register is now restored (see also word /6D4).

2910 The NAD Field disables the 8251 control signals and enables the 2901. Micro-inst CRTN enables a return to the main routine SENDAD.

ROUTINE SENDAD

The character is sent, so now the next character is isolated from Register A0. This principle is shown in the Flowchart of Figure 3.11F.
After 5 characters a return is made to MCL routine.

Address /685 Load /004 into Q

2901 The NAD Field has a value of /004 and Micro-inst LDQ is active to load this value into Register Q.

2932 Not significant

Address /686 Put the value of PC into Q

2932 The value of PC is fetched (FPC) and written onto the D lines (DE32).

2901 Operations DMQM1 and CARIN (defined in the control field bits 0-9) enable operation Q-4 (/000 - /004) giving a value of /FFFC. This new value is loaded into Q (LDQ).

2910 A CJP Micro-inst is executed enabling jump to the VISU Routine.

ROUTINE VISU (/602, /603)

Here the subroutine SEND DATA TO PANEL is executed the data is displayed and then the CPU stays in the Idle routine until an event occurs. The Idle Loop is shown in the Simplified Micro-instruction Chart at the beginning of the Micro Charts. The value /604 is inverted and loaded into R and Q.

Address /604 Take the next Micro-instruction address from PLAMAP.

2901 Normally the R2 Field of the Macro-instruction (bits 11-14) are reset however, in this case (starting-up) it is not significant.

2932 Not significant

2910 Signal PLAMAPN from the 2910 enables PLAMAP which gives the next address via the NAD lines. In this case the address given by PLAMAP on the NAD lines is as follows:

	NAD	0	1	2	3	4	5	6	7	8	9	10	11
Address	(38D)	0	0	1	1	1	0	0	0	1	1	0	1

This is the address of Interrupt (INT) or Idle; in this case it is Idle.

Address /38D

2901 Not significant

2932 Not significant

2910 Signal IRUNA is tested and the result TESTN indicates whether an interrupt is active or not. In this case there is no interrupt so the Microprogram goes to address /38E.

Address /38E Check the Flag which was set at address /603 during the routine VISU.

2932/2901 The Flag which was set in the Register R is written onto the D Lines with Micro-inst FR and DE32. At the ALU output the Flag is tested by condition D equal to Q (ALUZERO).

2910 After testing ALUZERO which = 1 in this case the next address is accessed with a CJP.

Address /5F2
  2901 Compare contents of register Q with value /604.
  2932 Not significant.
  2910 If ALUZERO go to address /604 because it is not necessary to execute subroutine SD and SENDAD again.

Address/604
  2901 Not significant
  2932 Not significant
  2910 Signal PLAMAPN from the 2910 enables PLAMAP via the NAD lines. In this case the address given by PLAMAP is /38D. These 4 addresses form the Idle Loop and the Micro program continues in this loop until an event occurs.

3.19.2 FLOWCHARTS

The flowcharts represent the microprogram known as "COSYN - P857R Remake (CP7A) - Index 1B - (PROM 0 thr. 6 / 12 NC: 641.1 thr. 647.1) d.d. 08.10.81".

Terms employed in the following flowcharts are:

/X : A hex number which is a constant.
(R1) : A number between ( ) indicates the register contents addressed; A1 for example.
BIO — DI : BIO content is loaded into the Data Input Buffer.
23 : Off page connector referring to figure 3.19.23.

Not all routines and subroutines are represented by a flowchart. On the next page a listing is made of included and not included routines.

FIGURE NUMBER	NUMBER OF ROUTINE(S)	INCL.	NOT INCL.
3.19.1a	IDLE LOOP	X	
3.19.1b	RSL, MCL, STAT, VISU	X	
3.19.2	CLEAR, AUTO RESTART	X	
3.19.3	DECOPUP	X	
3.19.4	RR, LA, MLM2	X	
3.19.5	RM1, RM2, LM1, USEZO USERET	X	
3.19.6	INST, RUN, CPINT, LR RST, PREAL	X	
3.19.7	PRCC, LDSP, PWR, POFF, RPA	X	
3.19.8	PANEL IPL, PRESET	X	
3.19.9	PUPITRE, PUP	X	
3.19.10	MICRODIAGNOSTICS, (TEST K, PLAVEC, PLACR, CR, DI/DO AND BUS LINES, ERR1)	X	
3.19.11	MICRODIAGNOSTIC (TEST DI/DO AND BUS LINES, TEST MEMORY	X	
3.19.12	MICRODIAGNOSTIC (TEST V24, TRAPOK, TRAPER, COMRZO, END)	X	
3.19.13	MICRODIAGNOSTICS (TEST MIOP)	X	
3.19.14	MICRODIAGNOSTIC (TEST MIOP - cntd)	X	
3.19.15	INTERRUPT, PAF, SAVE, INHSAVE	X	
3.19.16	CALLM, TRAPMAP, TRAPS PLAMAP AND PLAVEC	X	
3.19.17	TRAPVEC, TRAPS, DSET	X	
3.19.18	SENDAD, TSOC, WAIT	X	
3.19.19	SD, TROC, ROC, WAITST	X	
3.19.20	SEND COMMAND TO 8251	X	
3.19.21	VISUAD, VISUL, RUNIR	X	
3.19.22	SDV24, SCV24	X	
3.19.23	FETCH, ECLAT, PAFTCH, PAFW2, REZ (CR)	X	

FIGURE NUMBER	NAME OF ROUTINE(S)	INCL.	NOT INCL.
3.19.24a	ADDRESSING ROUTINES RT2 THR. 7	X	
3.19.24b	ADDRESSING ROUTINES RT2A THR. 7A	X	
3.19.25	ADDRESSING ROUTINES RT3S THR. 7S	X	
3.19.26	OPCODE 0: LDPR, LDPRP, LDR, STR, STPR		X
3.19.27	OPCODE 0: LDK, LDR, LDKP, LD, LDP, ST, STP	X	
3.19.28	OPCODE 1: AB, ABR, ABPR, ABL		X
3.19.29	OPCODE 2: ADK, ADR, ADKP, ADQRP, ADPR, AD, ADP. ADS, IM		X
3.19.30	OPCODE 3: SUK, SUR, SUPR, SUPRP, NGR, NGPR, SURP, SUXP		X
3.19.31	OPCODE 3: SU, SUP, SUS, C2		X
3.19.32	OPCODE 4: ANK, ANPR, ANR, TMR, TMPR, AN, ANS, CM		X
3.19.33	OPCODE 4: HLT, INH, RIT	X	
3.19.34	OPCODE 5: ORK, ORPR, ORR, LKM, ENB, OR, ORS		X
3.19.35	OPCODE 6: XRK, XRPR, XRR, XR, XRS, TNM, TNMP		X
3.19.36	OPCODE 7: SLL, SRL, STRC, SRA		X
3.19.37	OPCODE 7: DRN, SRN, DLA		X
3.19.38	OPCODE 7: DLL, DLC, DRL, DRC, DRA		X
3.19.39	OPCODE 7: SLA, SLN, SLC		X
3.19.40	OPCODE 7: MS, DLN		X
3.19.41	OPCODE 7: MLR, MLK		X
3.19.42	OPCODE 7: ML		X
3.19.43a	OPCODE 7: TL, TS	X	
3.19.43b	OPCODE 7: MSR (refer to fig. 3.19.16)		X
3.19.44	OPCODE 8: FO, FOS, FLD, FST,		X
3.19.45	OPCODE 8: CIO/OTR	X	
3.19.46	OPCODE 8: V24 STATES	X	

FIGURE NUMBER	NAME OF ROUTINE(S)	INCL.	NOT INCL.
3.19.47	OPCODE 8 : CIO HALT V24, RSTV24, SSTFLO, RAD	X	
3.19.48	OPCODE 8 : OTR-V24	X	
3.19.49	OPCODE 8 : CIO/OTR EXTERNAL DEVICE INR/SST, TST EXTERNAL DEVICE	X	
3.19.50	OPCODE 8 : MUR, MUPR, MU		X
3.19.51	OPCODE 8 : TSB, TSBR		X
3.19.52	OPCODE 9 : FFL, FFX		X
3.19.53	OPCODE 9 : INR, SST, TST (V24), INRV24, ECHO	X	
3.19.54	OPCODE 9 : SSTV24	X	
3.19.55	OPCODE 9 : DIVIDE		X
3.19.56	OPCODE 9 : TRB, TRBR OPCODE 10: TB, TBR, EL, ES		X X
3.19.57	OPCODE 10: RF OPCODE 11: RB	X X	
3.19.58	OPCODE 10: DAR, DAK, DAPR, DA		X
3.19.59	OPCODE 11: DSPP, DSR, DS, DSK		X
3.19.60	OPCODE 12: SC, LC, ECFR, ECR, LCK		X
3.19.61	OPCODE 13: COS		X
3.19.62	OPCODE 13: MOA, COA		X
3.19.63	OPCODE 13: MOS, SITRT, FLAG		X
3.19.64	OPCODE 13: CC, CCK, CWP, CWPRP, CWP, CWPR		X
3.19.65	OPCODE 14: WER	X	
3.19.66	OPCODE 14: WER (CONT'D)	X	
3.19.67	OPCODE 14: MVF, MVSU, SUBQR2Z		X
3.19.68	OPCODE 14: EXR, EX, LDA, LDPA		X
3.19.69	OPCODE 14: CF, CFI, CFR, CFPR		X
3.19.70	OPCODE 14: RTN, (A1-A15)	X	
3.19.71	OPCODE 15: C1R, C1PR, C1, C1S, C1PS		

FIGURE NUMBER	NAME OF ROUTINE(S)	INCL.	NOT INCL.
3.19.72	OPCODE 15: RER		X
3.19.73	OPCODE 15: MVB		X
3.19.74	OPCODE 15: MVUS		X

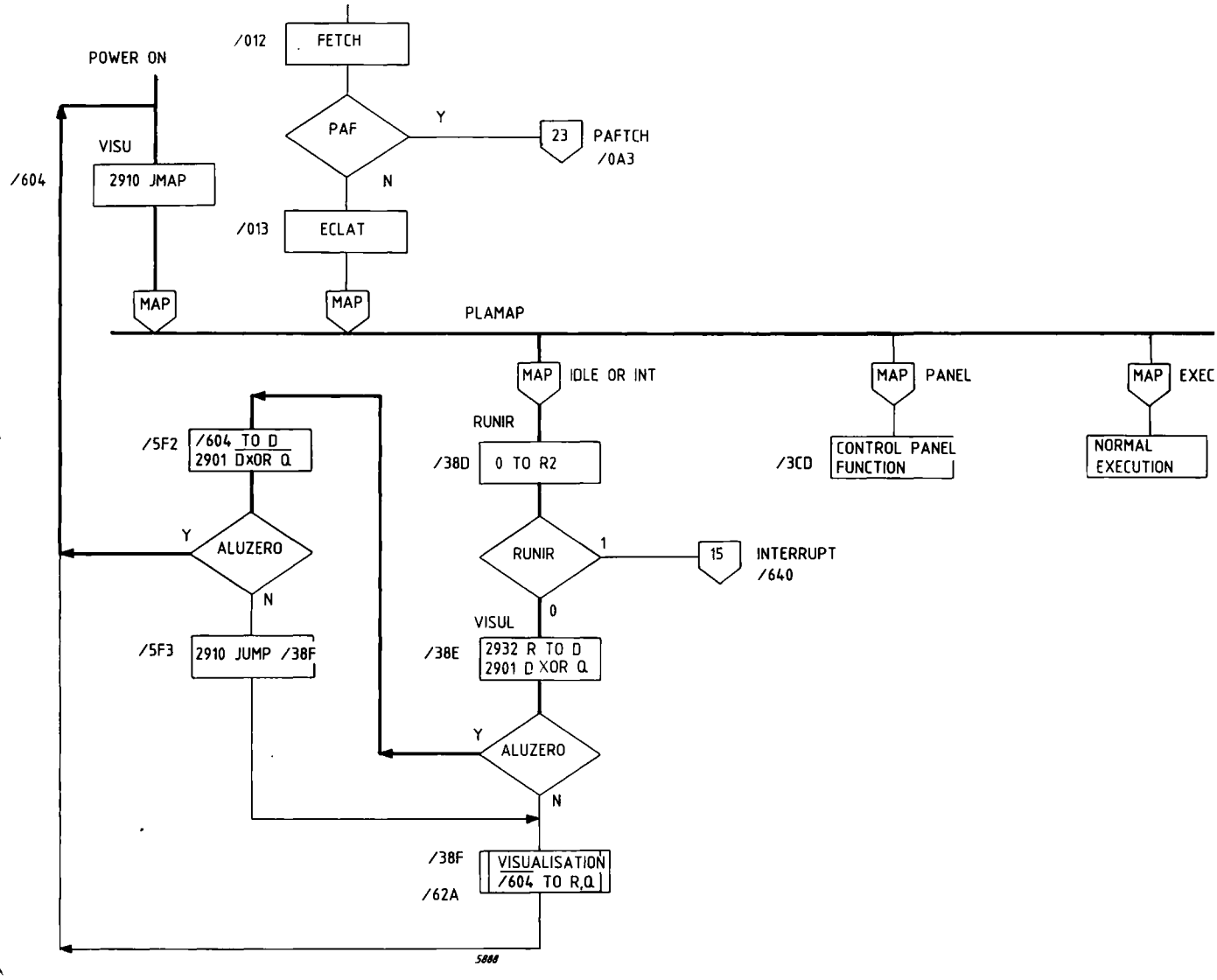


Figure 3.19.1a IDLE LOOP

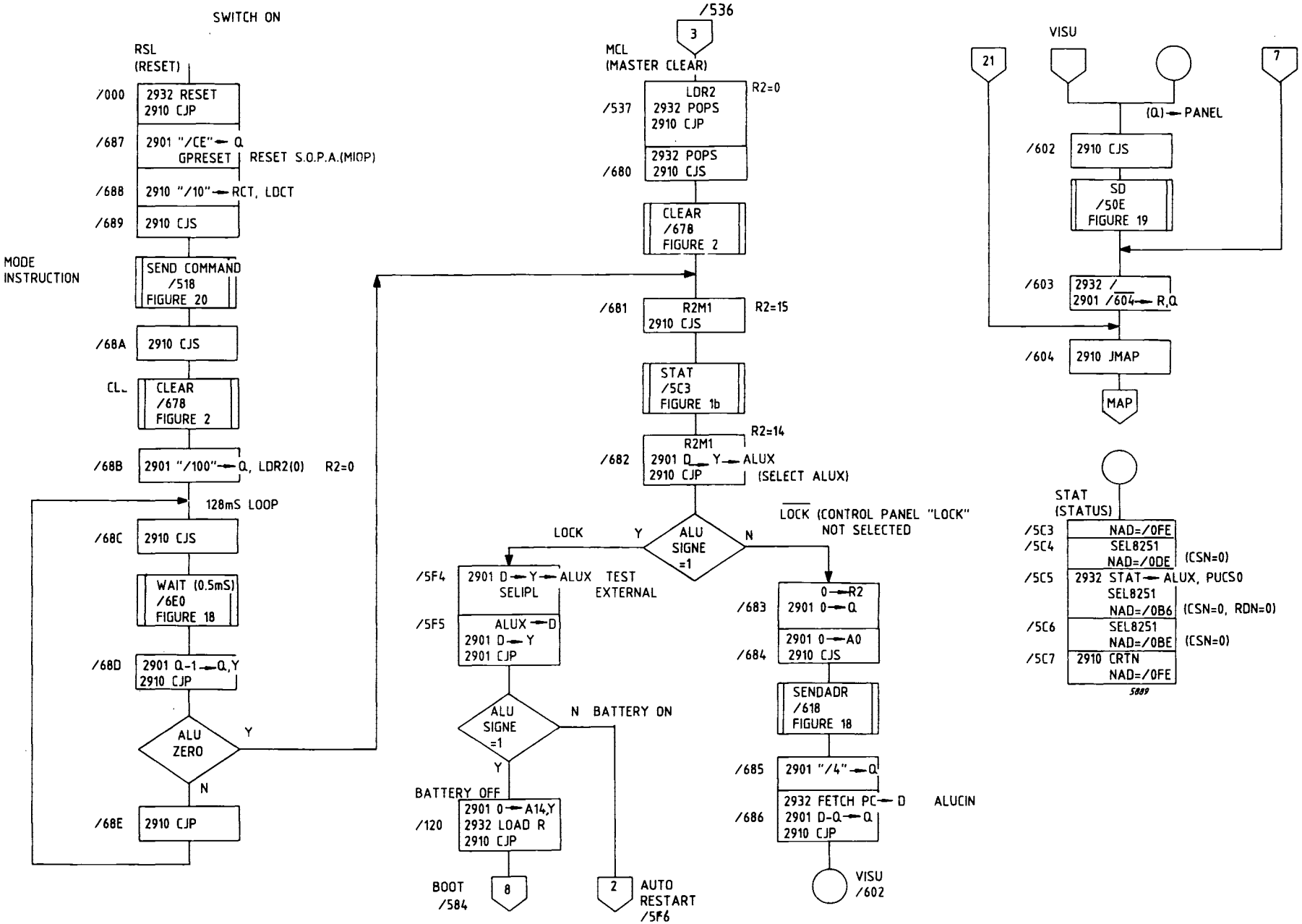


Figure 3.19.1b RLS, MCL, STAT, VISU

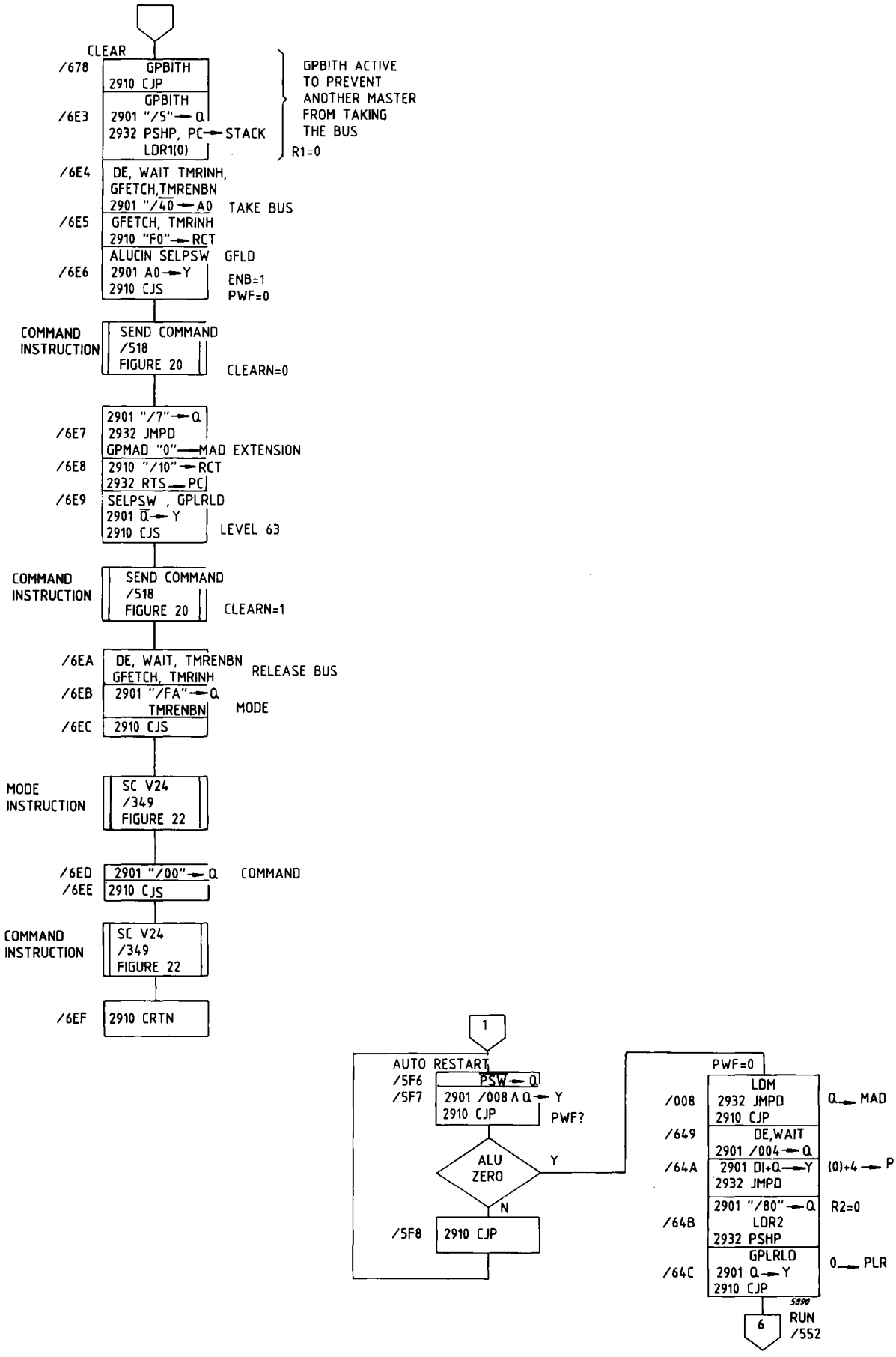


Figure 3.19.2 CLEAR, AUTO RESTART

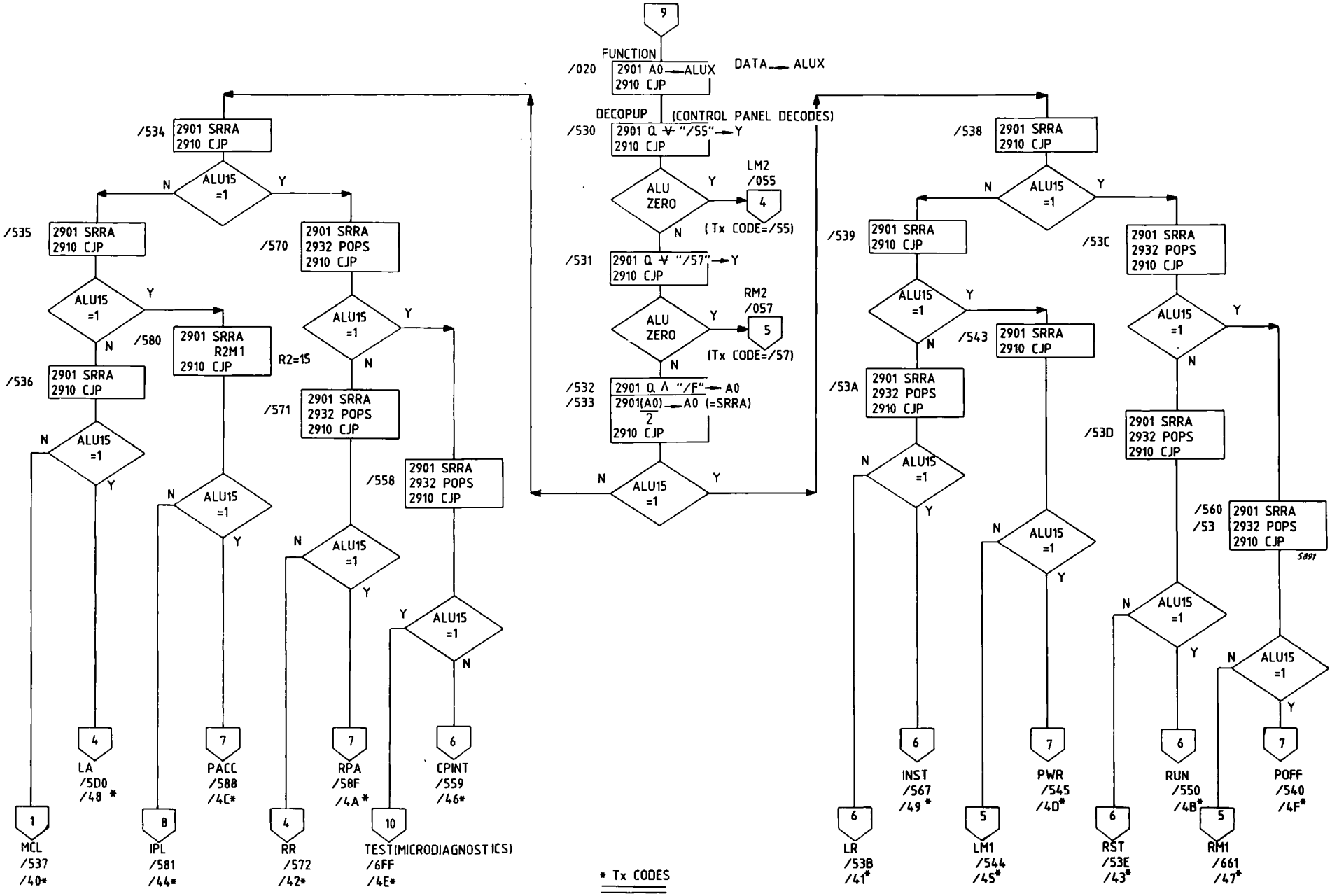
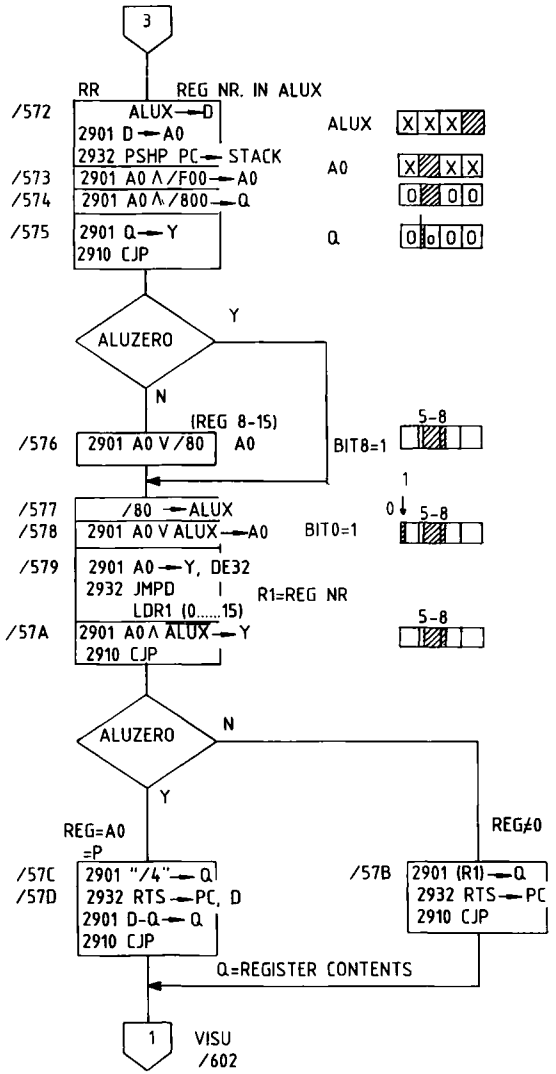
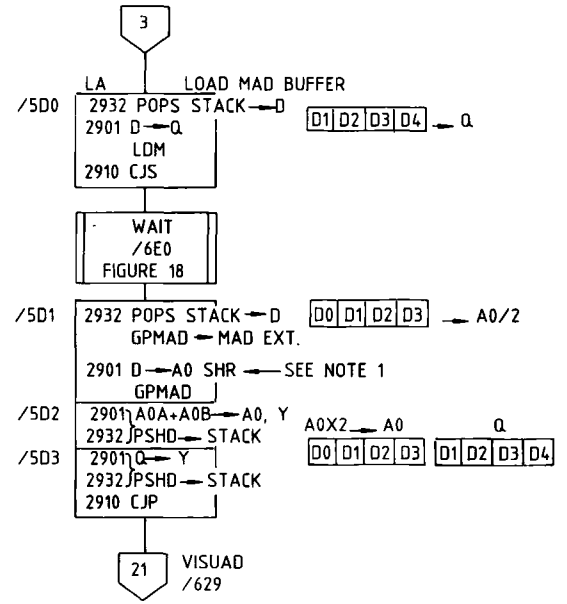
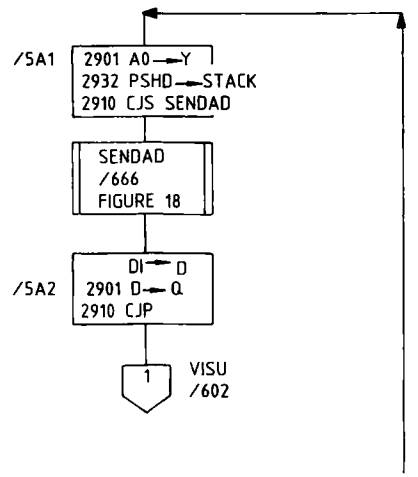


Figure 3.19.3 DECOPUP





NOTE 1 SHR ENABLES ALU17 TO LOAD
MADS EXTENDED
A0 BITS4-15 ARE DO NOT CARE



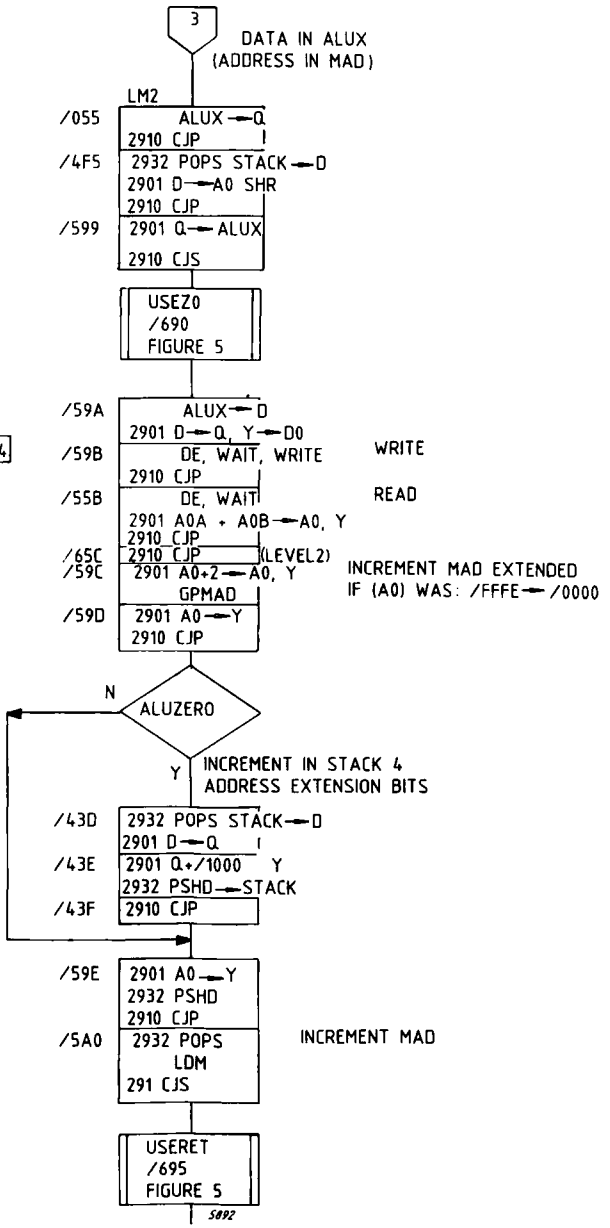


Figure 3.19.4 RR, LA, MLM2

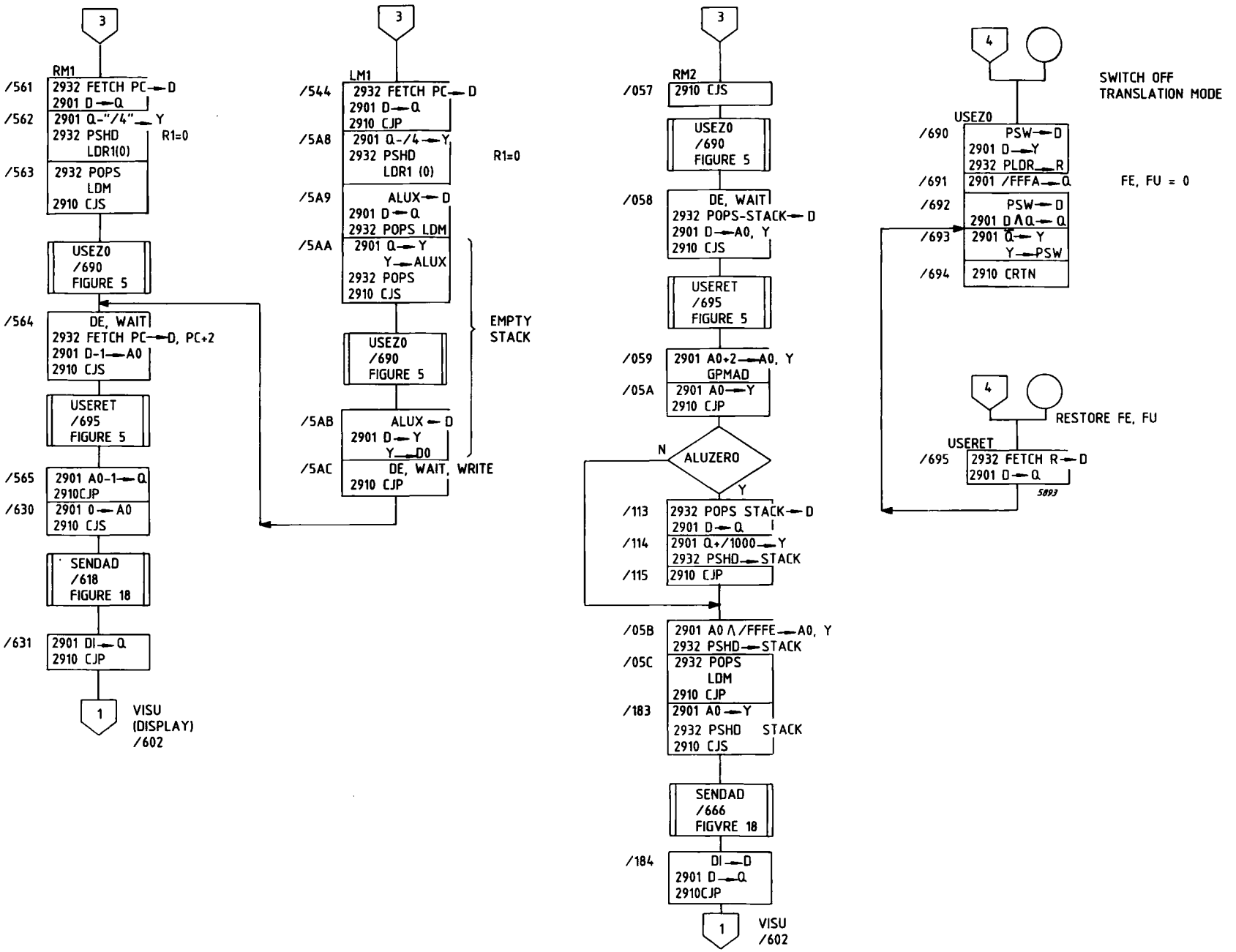


Figure 3.19.5 RM1, RM2, LM1, USEZ0, USERET

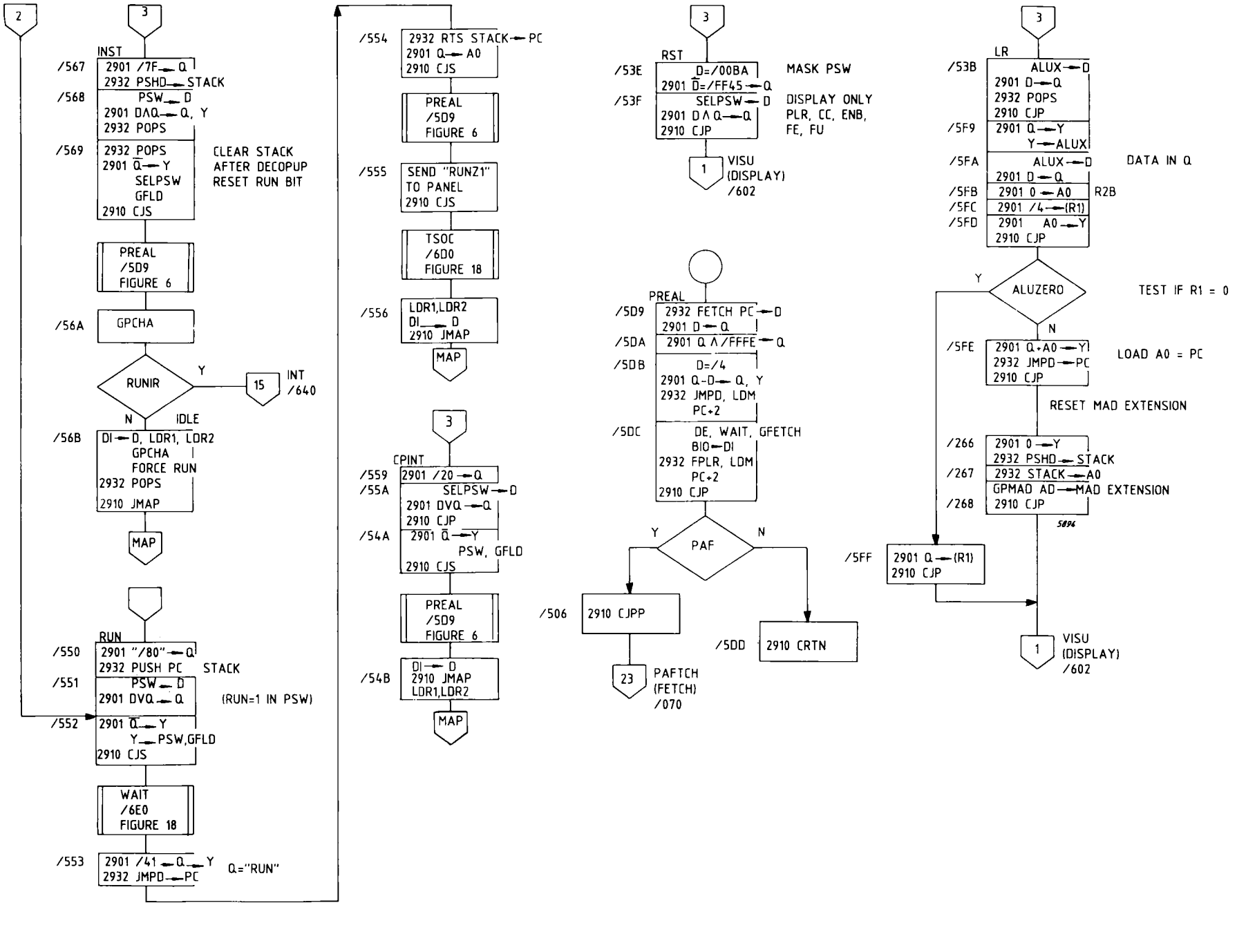


Figure 3.19.6 INST, RUN, CPINT, LR, RST, PREAL

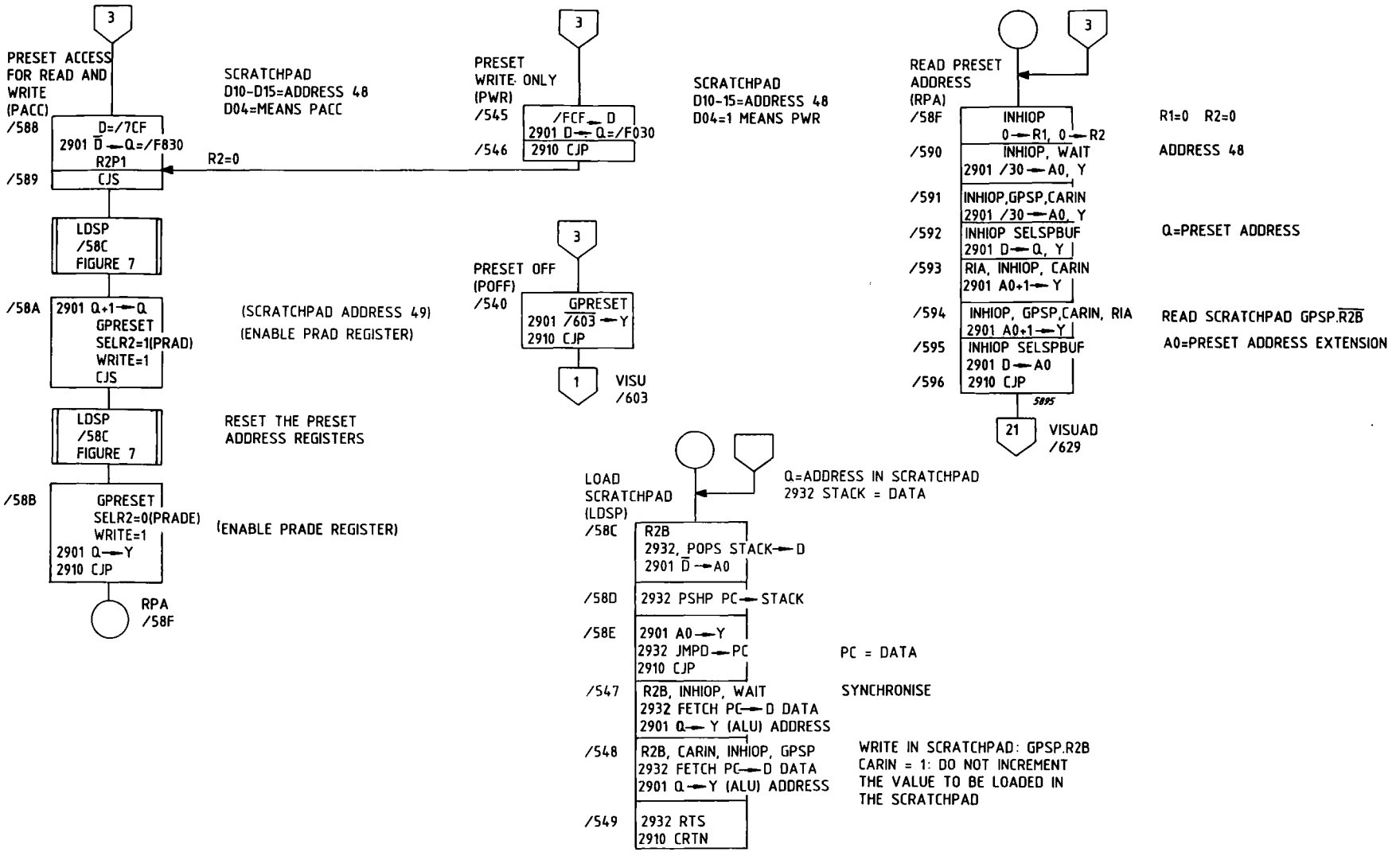


Figure 3.19.7 PRCC, LDSP, PWR, POFF, RPA

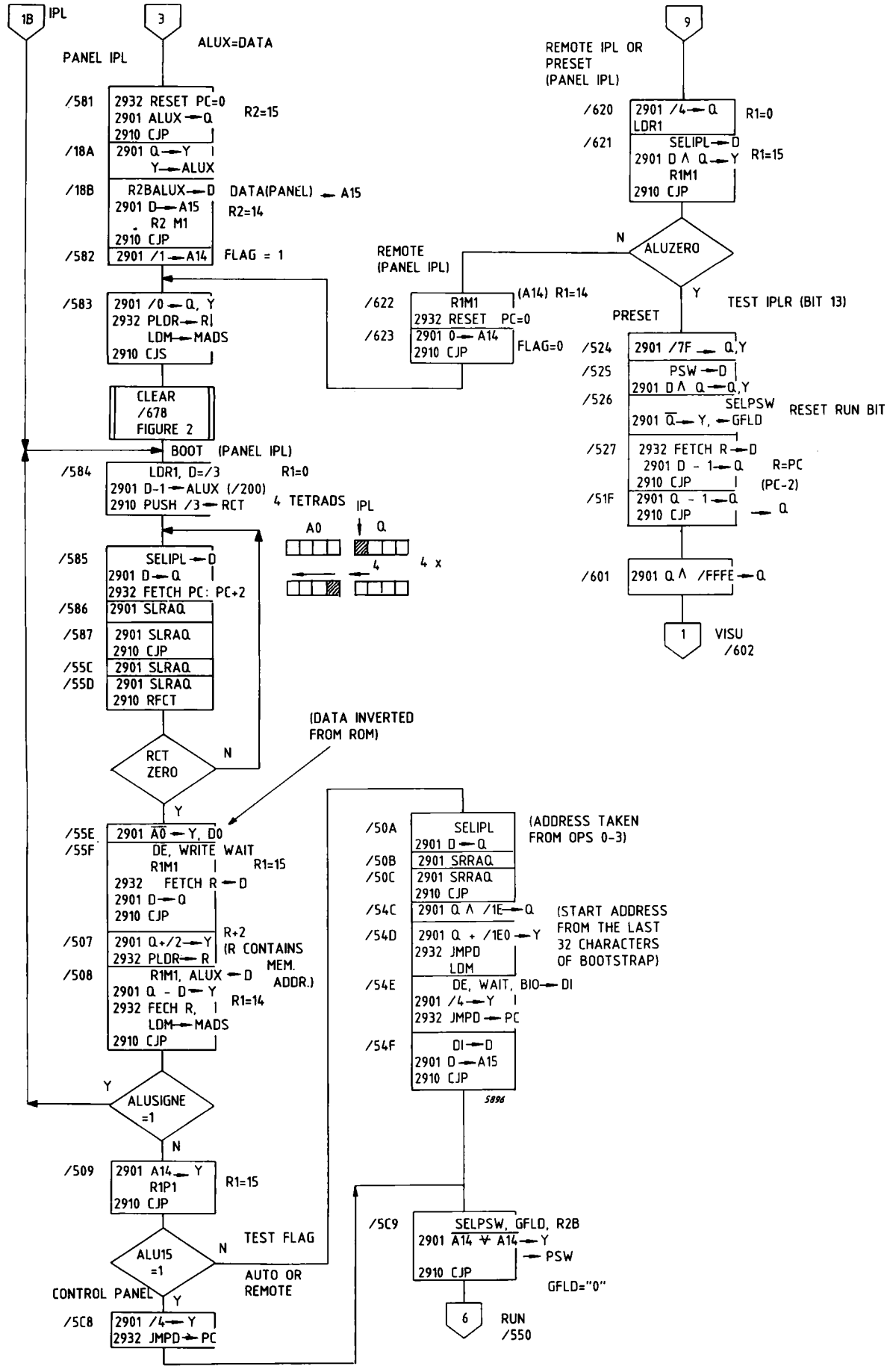


Figure 3.19.8 PANEL IPL, PRESET

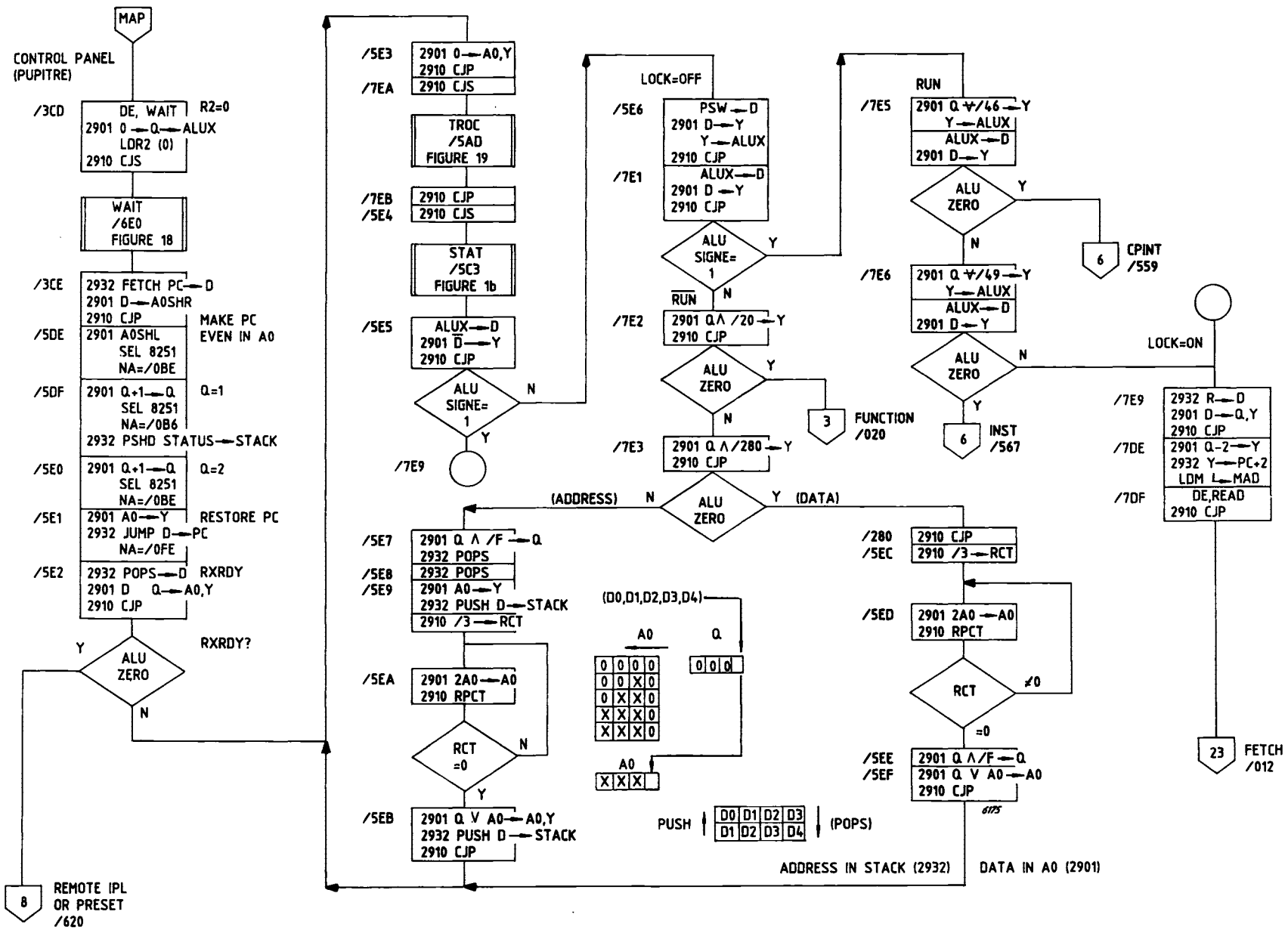


Figure 3.19.9 PUPITRE, PUP (LEVEL 2)

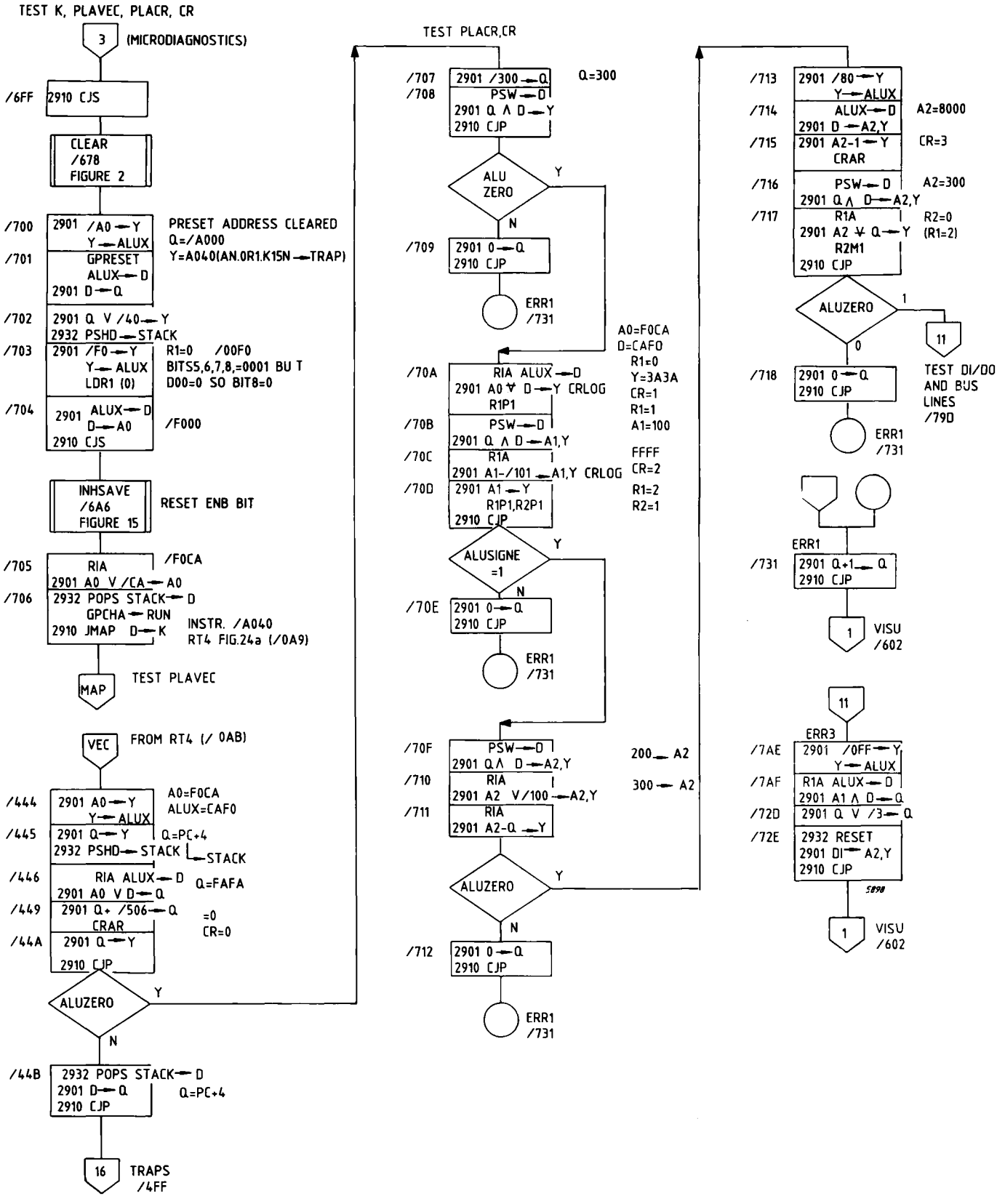


Figure 3.19.10 MICRODIAGNOSTICS, (TEST K, PLAVEC, PLACR, CR, DI/DO AND BUS LINES ERR1)

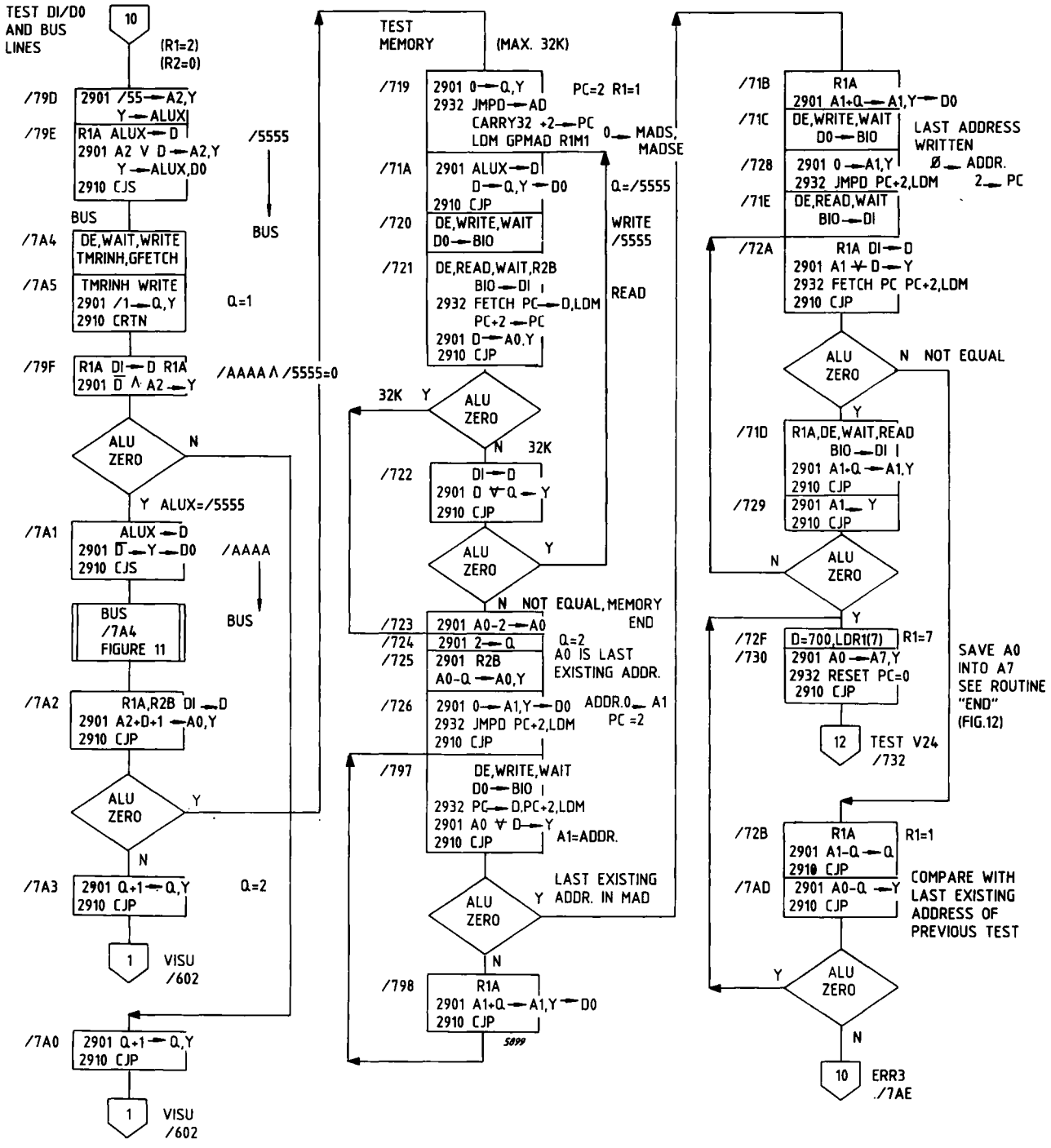


Figure 3.19.11 MICRODIAGNOSTICS (TEST DI/DO AND BUS LINES, TEST MEMORY)

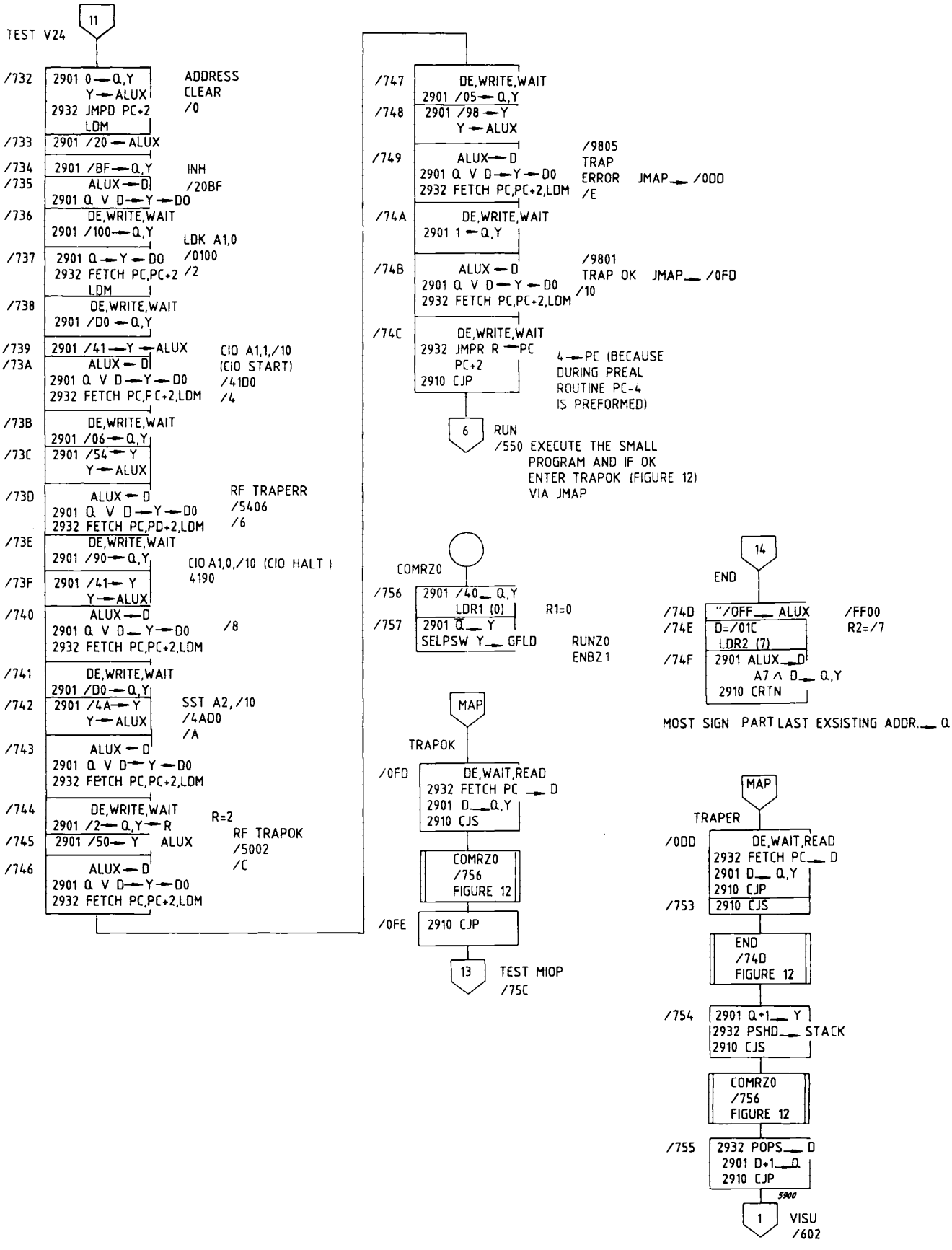


Figure 3.19.12 MICRODIAGNOSTICS (TEST V24, TRAPOK, TRAPER, COMRZO, END)

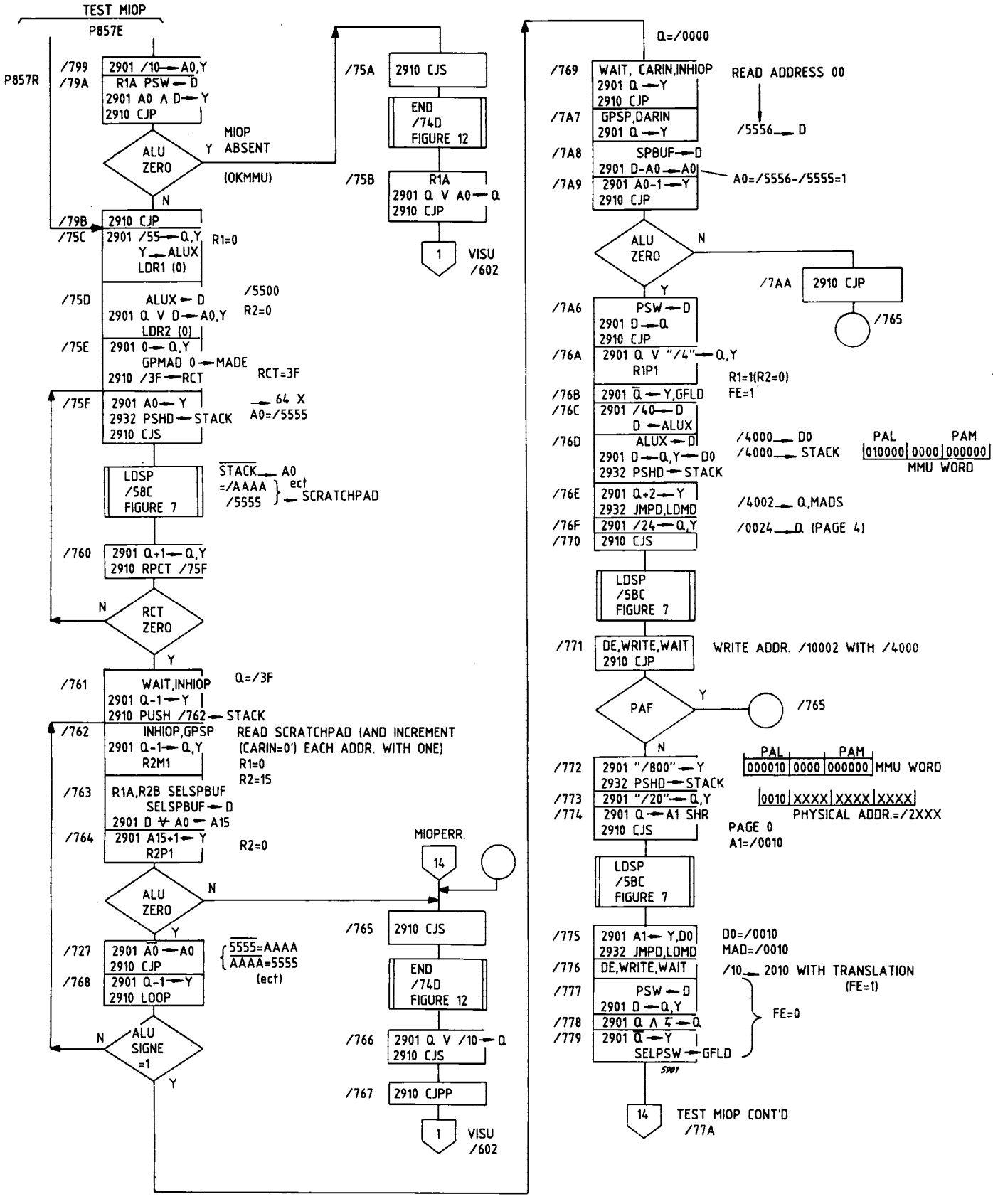


Figure 3.19.13 MICRODIAGNOSTICS (TEST MIOP)

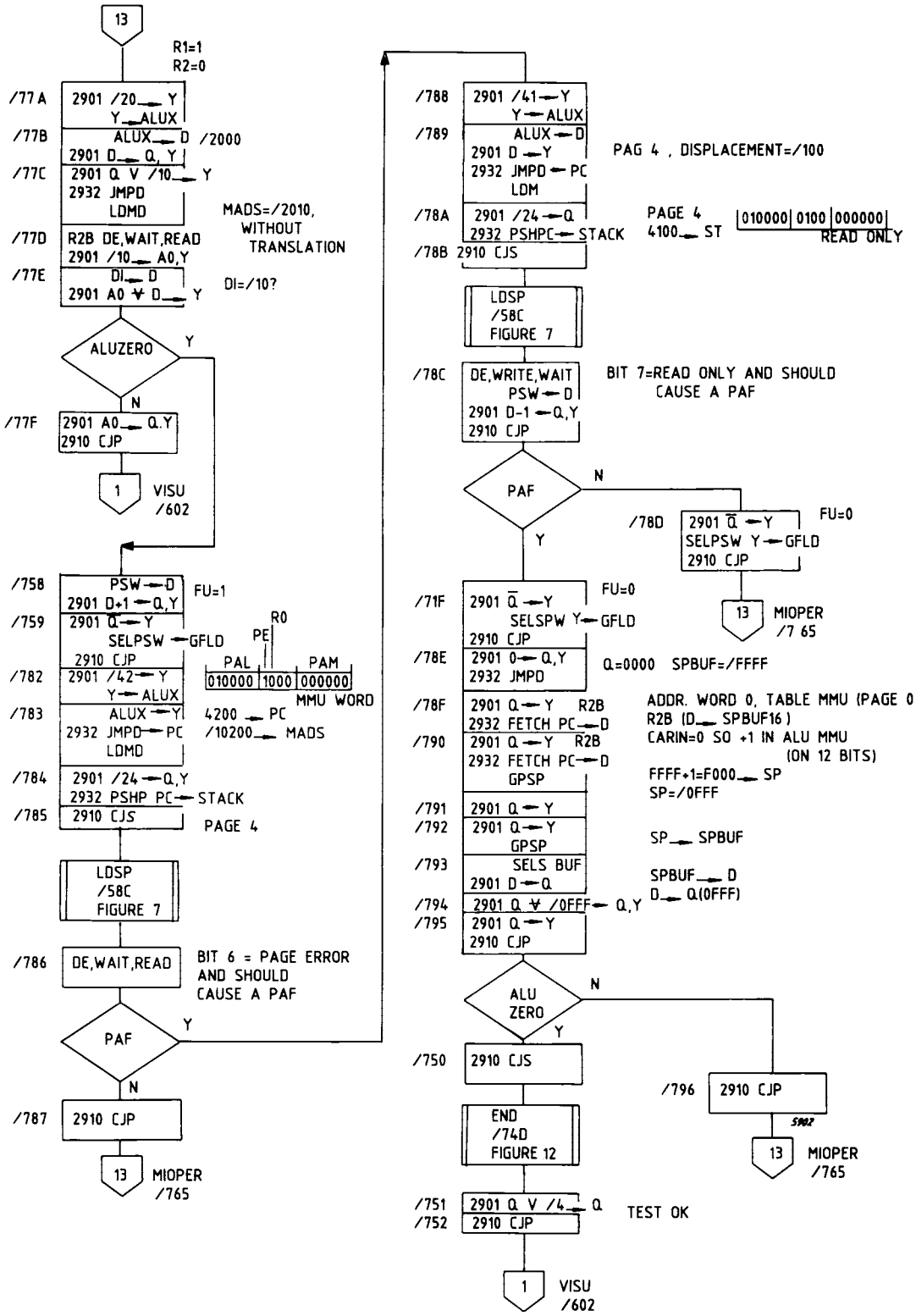


Figure 3.19.14 MICRODIAGNOSTIC (TEST MIOP - cntd)

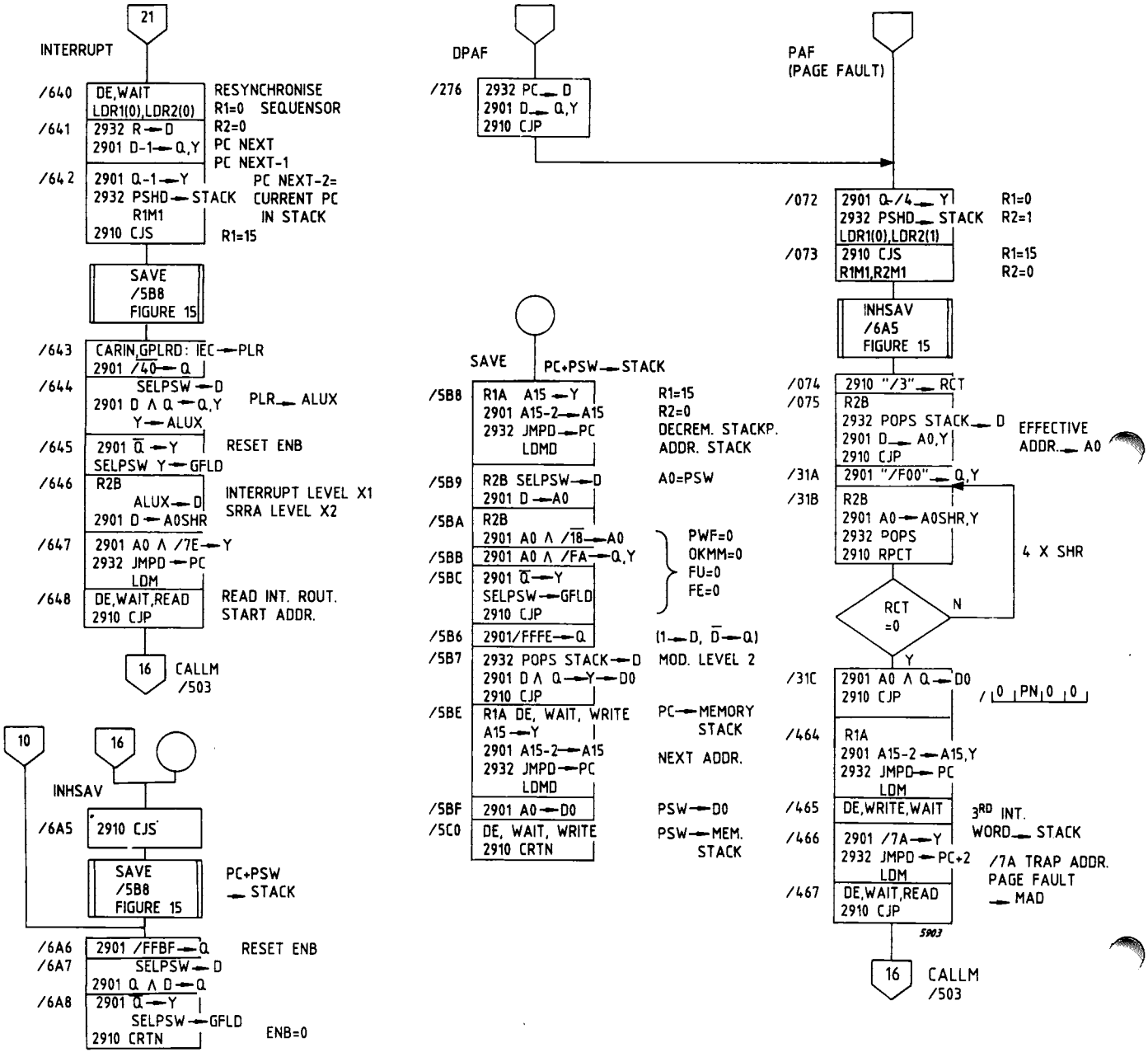


Figure 3.19.15 INTERRUPT, PAF, SAVE, INSHAVE

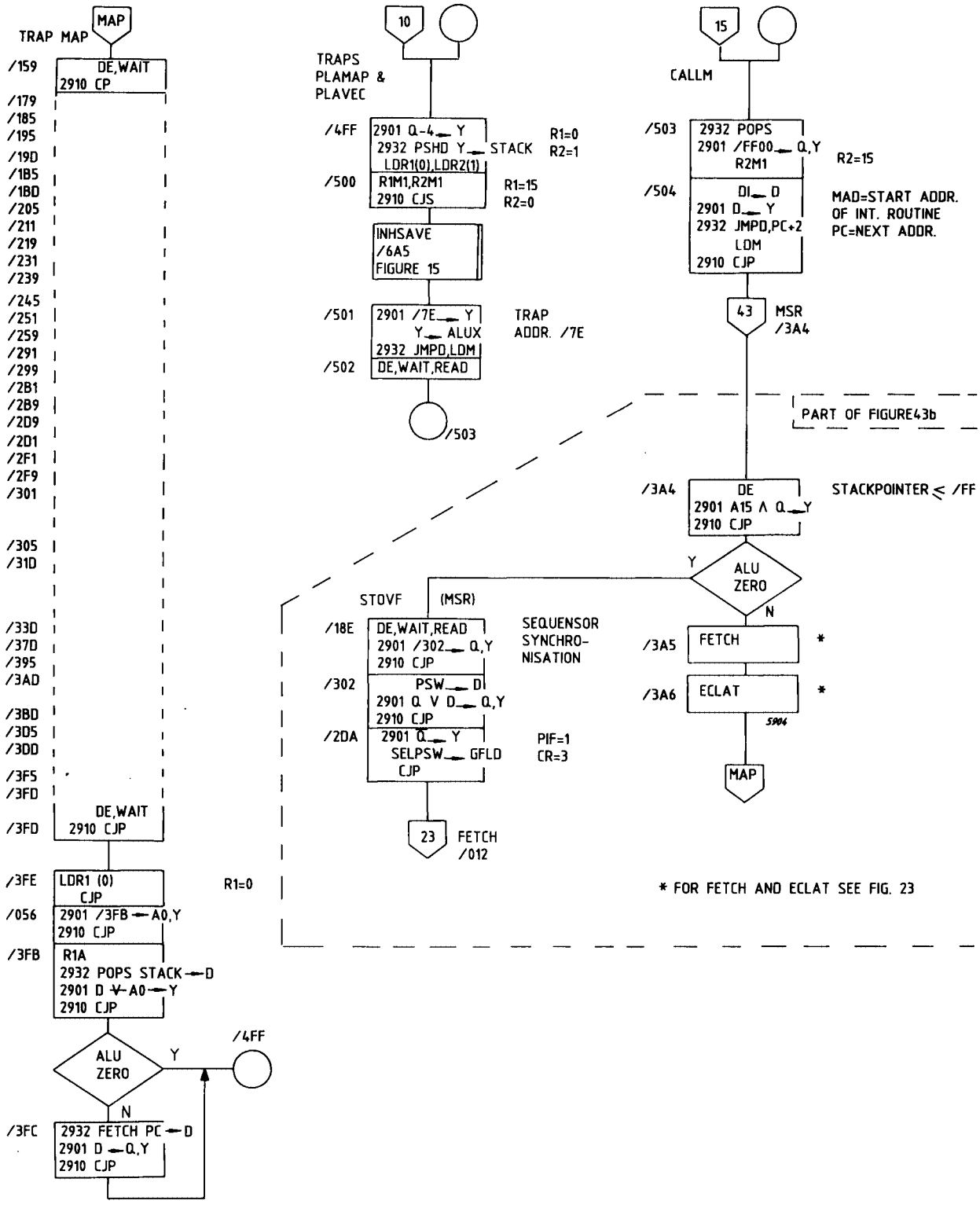


Figure 3.19.16 CALALM, TRAPMAP, TRAPS PLAMAP AND PLAVEC

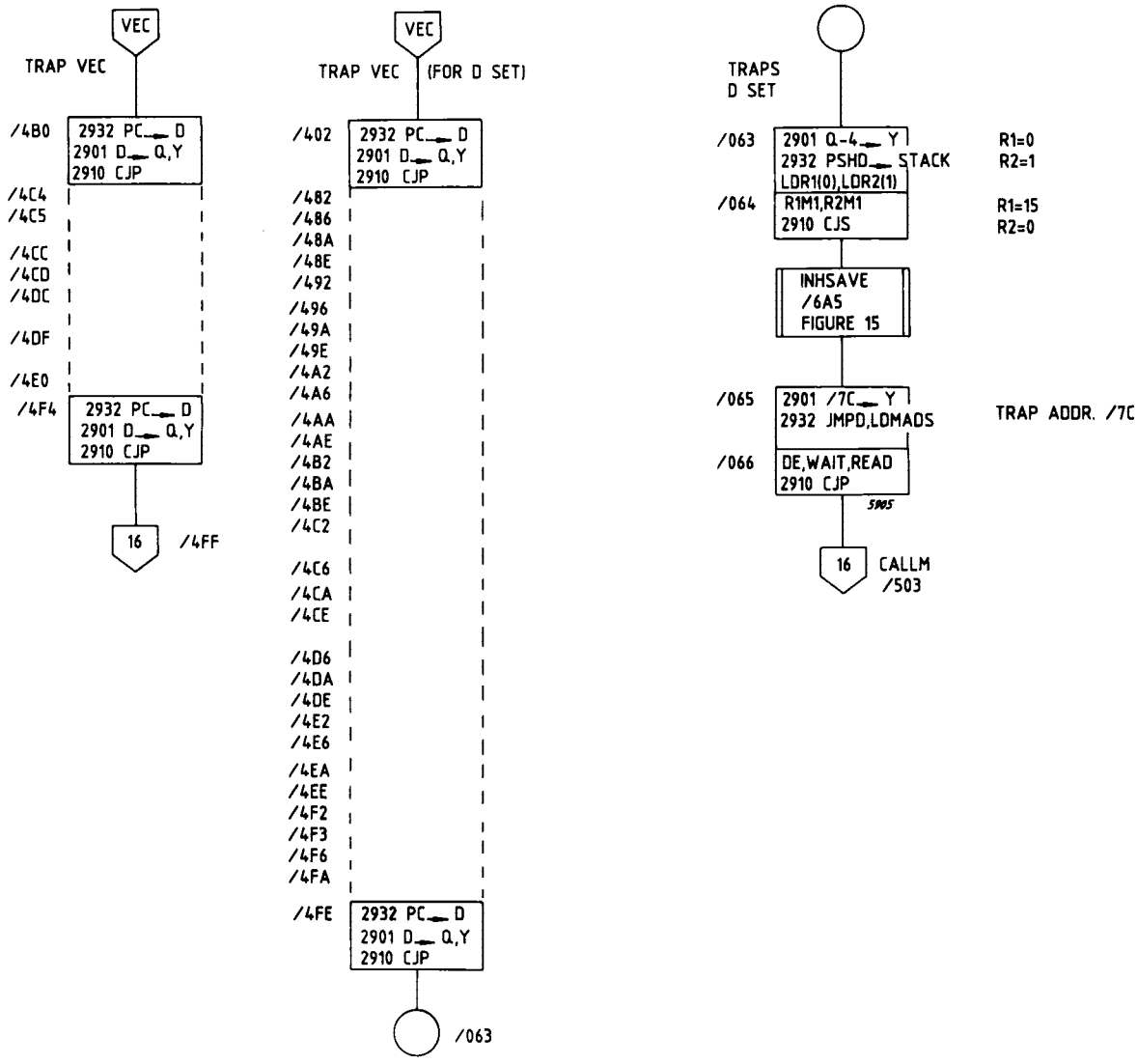


Figure 3.19.17 TRAPVEC, TRAPS, DSET

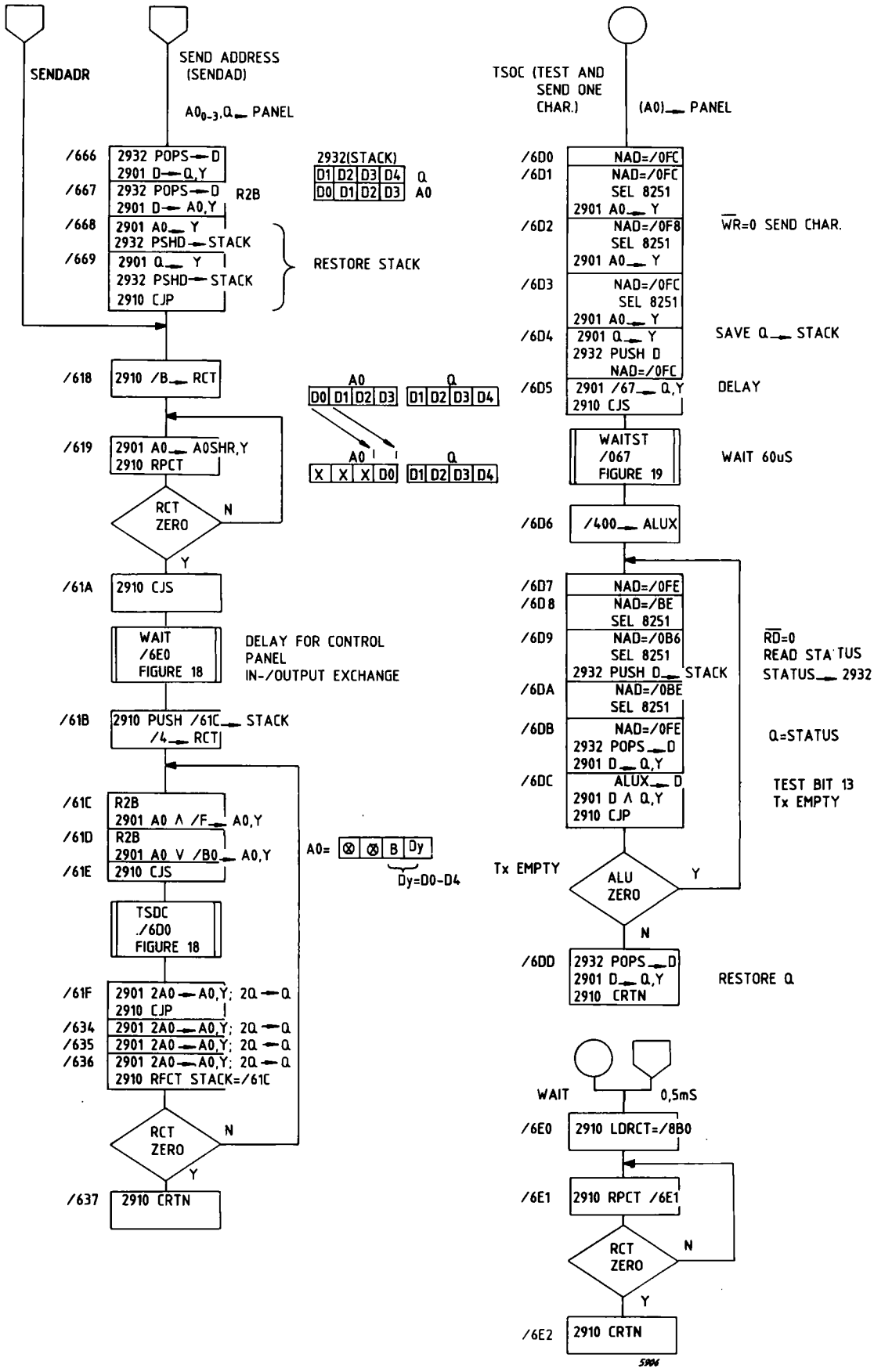


Figure 3.19.18 SENDAD, TSOC, WAIT

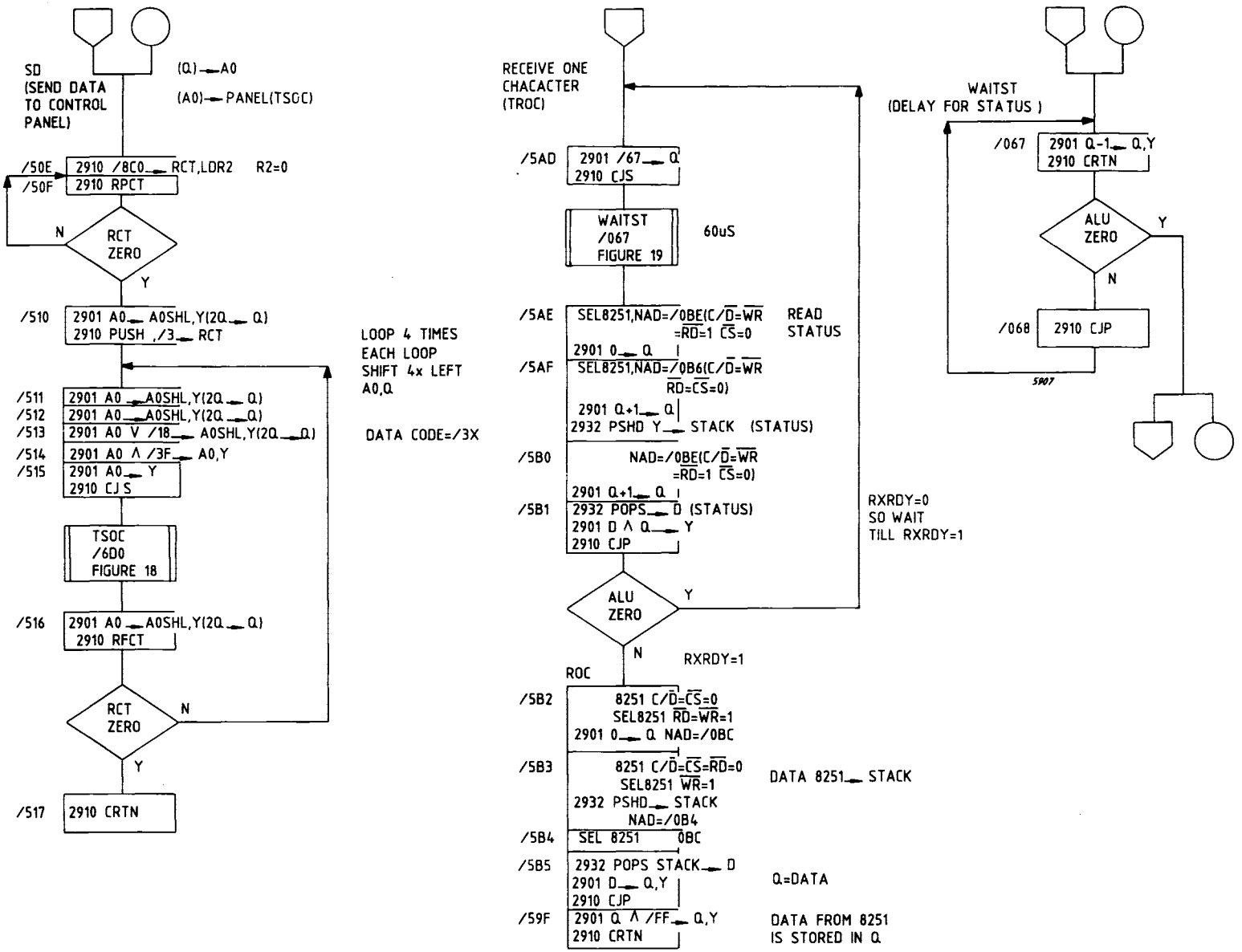
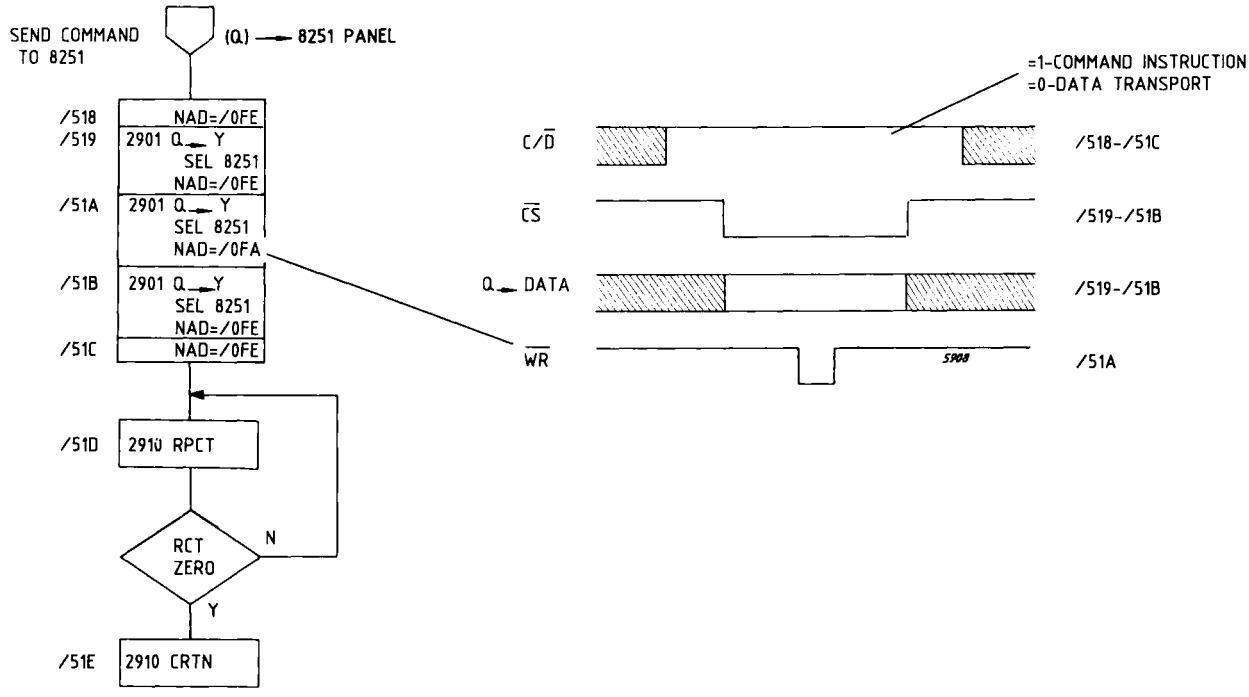


Figure 3.19.19 SD, TROC, ROC, WAITST



NOTE: BEFORE THE START OF THIS ROUTINE
Q ALREADY CONTAINS EITHER THE
MODE OR COMMAND INSTRUCTION

Figure 3.19.20 SEND COMMAND TO 8251

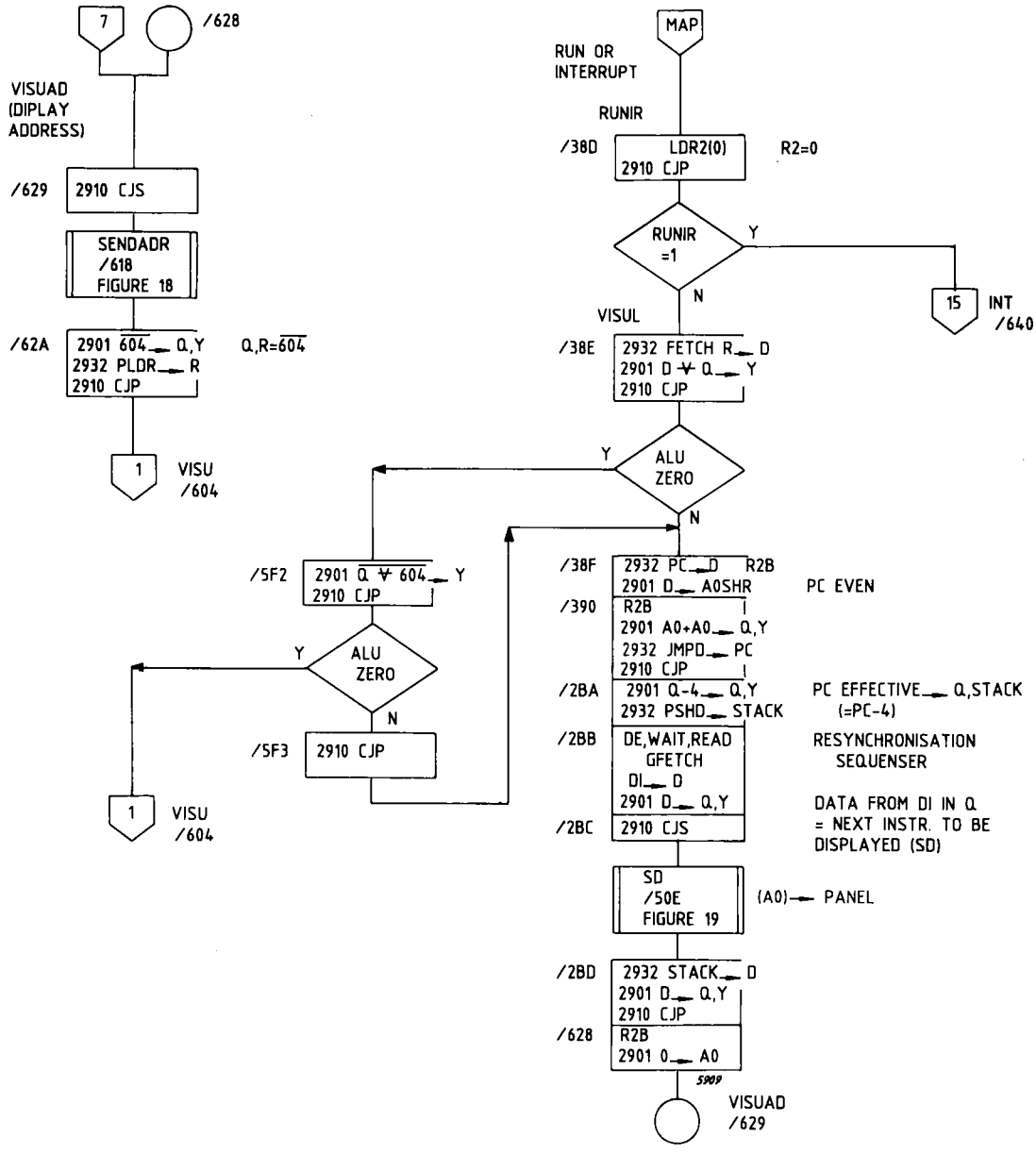


Figure 3.19.21 VISUAD, VISUL, RUNIR

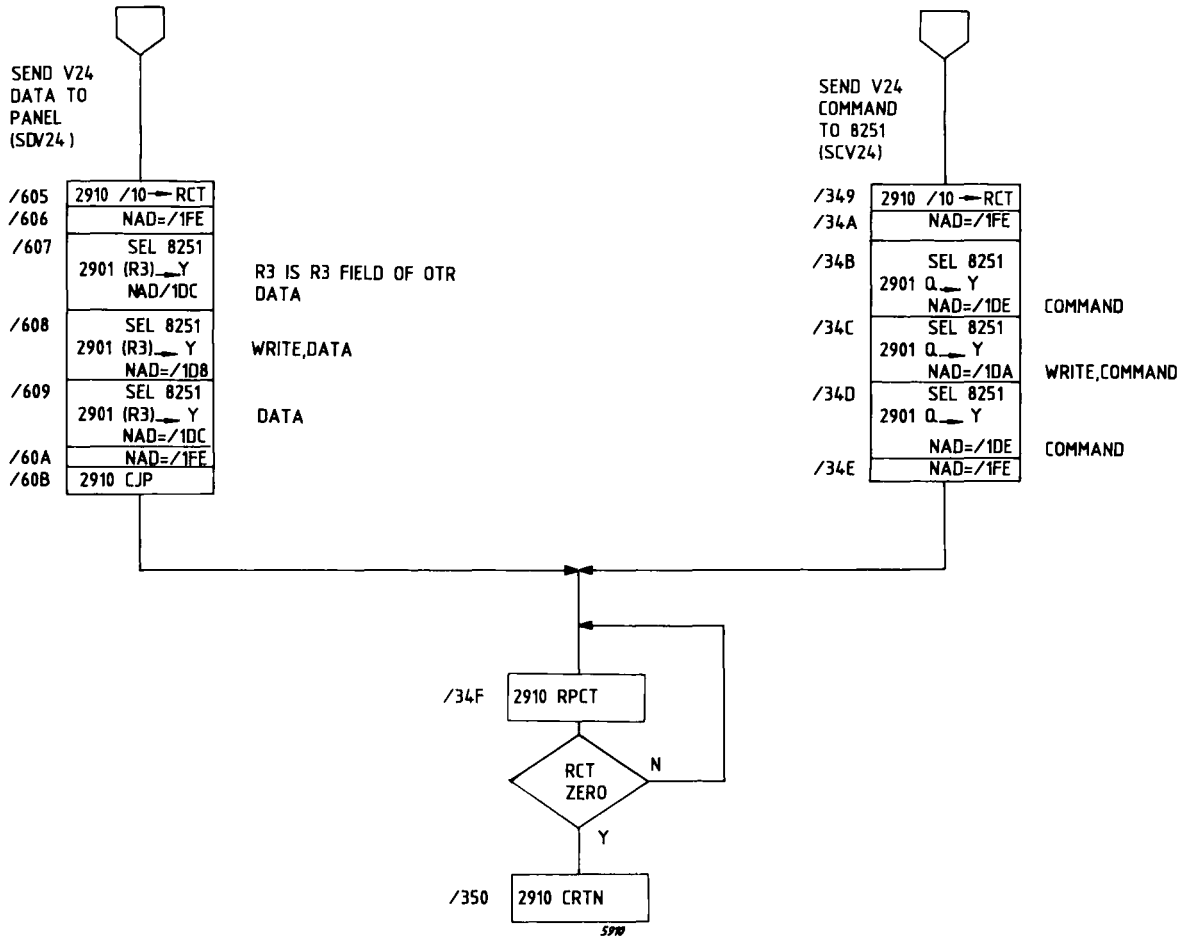


Figure 3.19.22 SDV24, SCV24

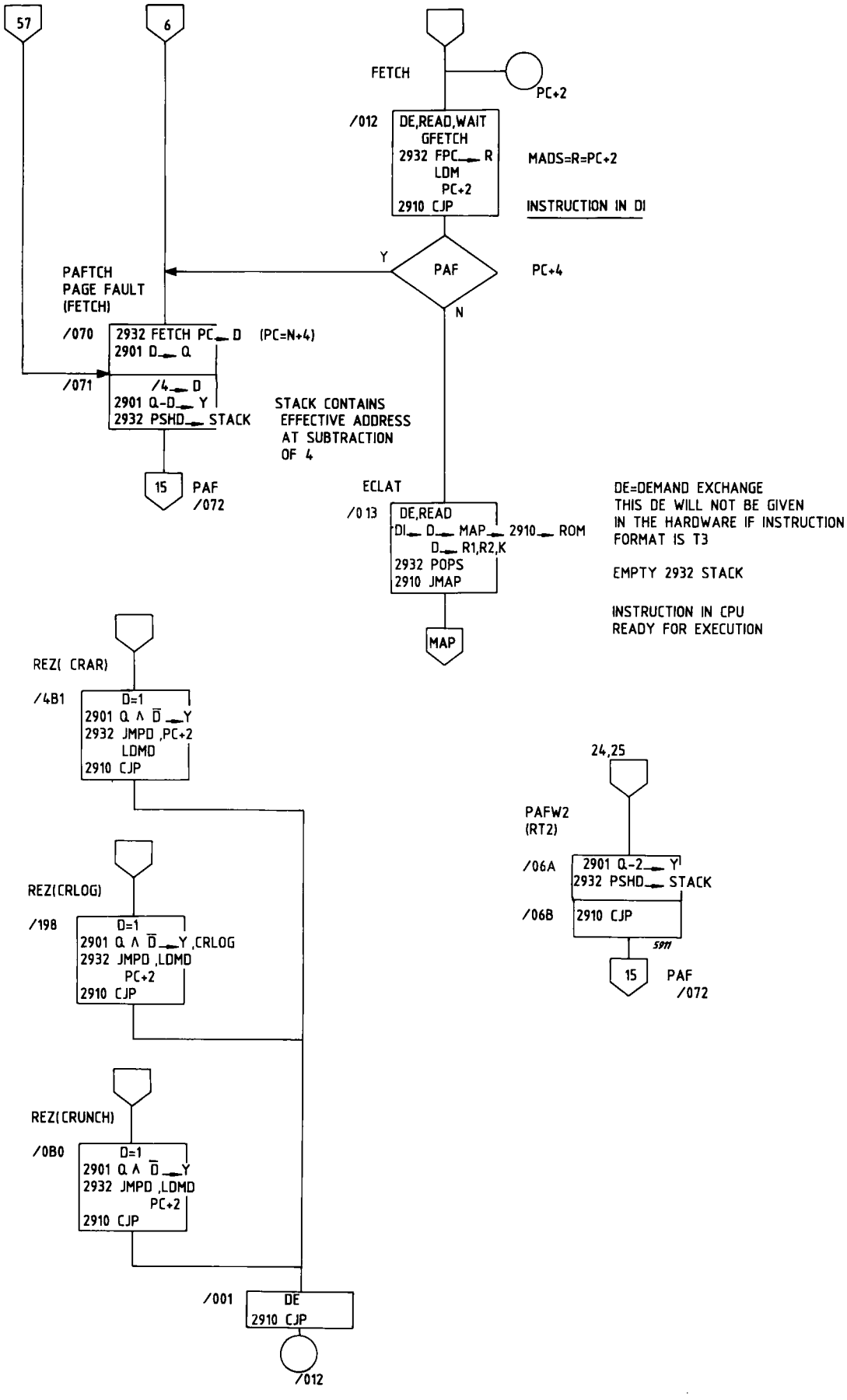


Figure 3.19.23 FETCH, ECLAT, PAFTCH, PAFW2, REZ (CR)

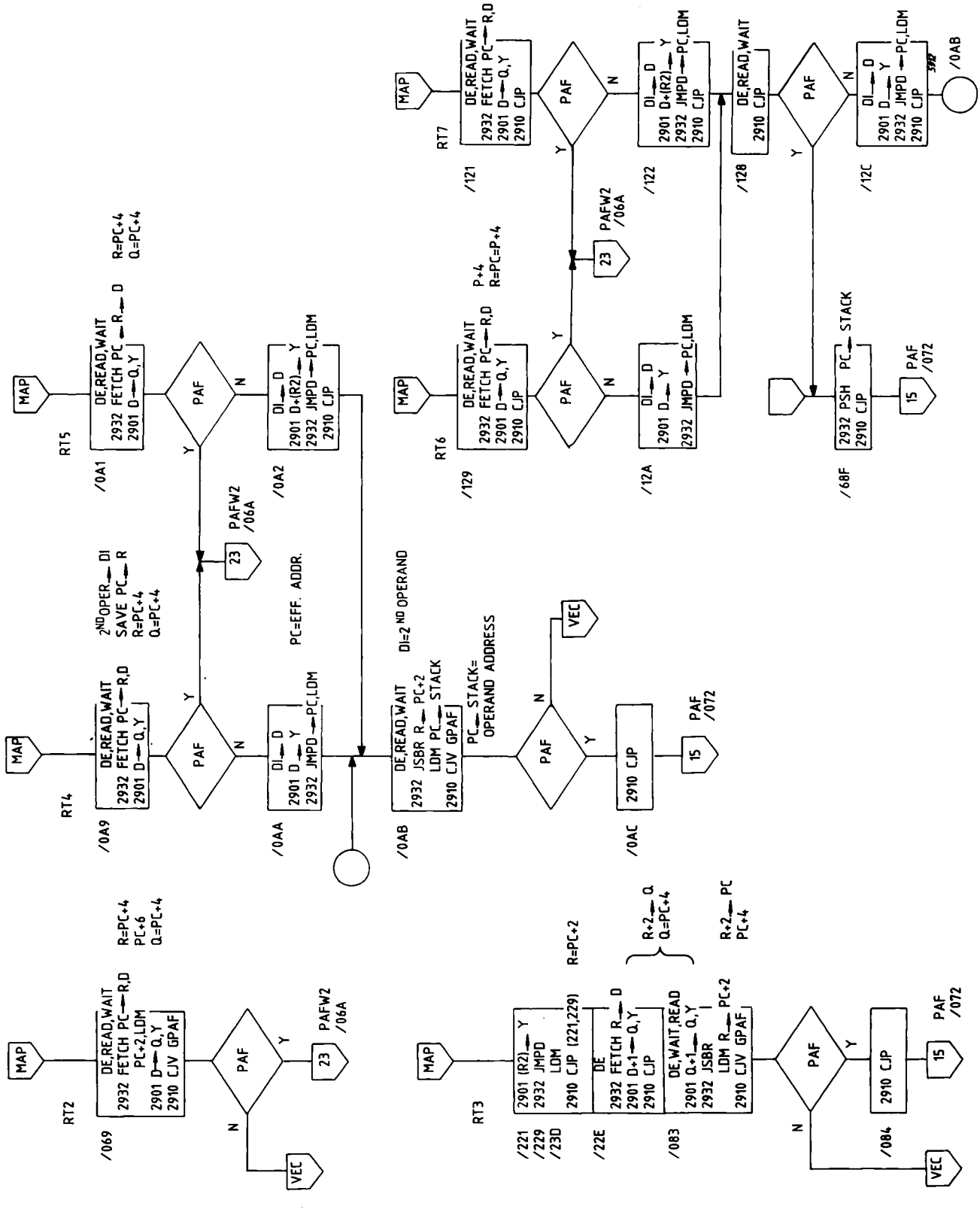
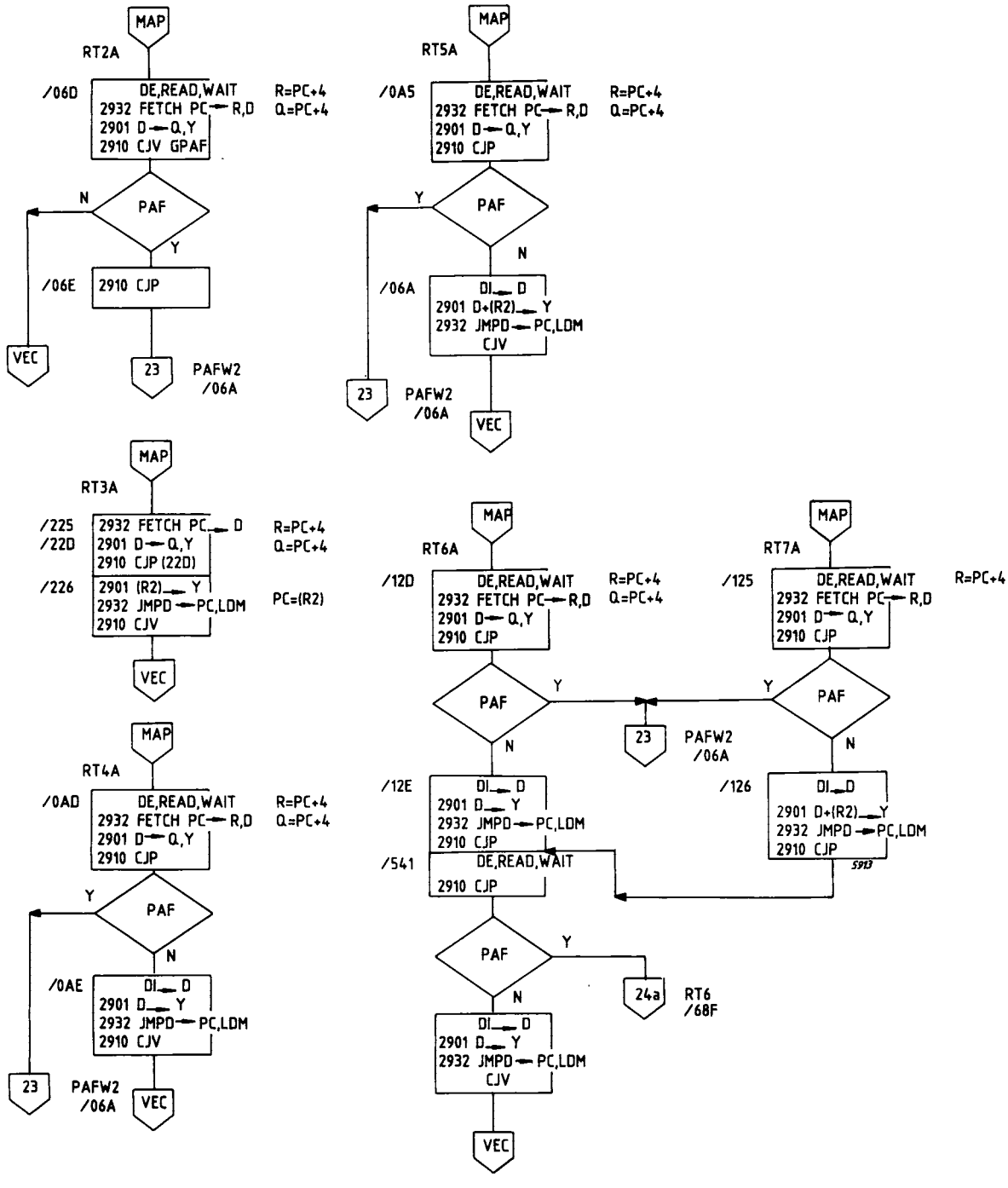


Figure 3.19.24a ADDRESSING ROUTINES RT2 THR. 7



NOTES: RT2A: USED FOR LCK,CCK,CWK,CWKP, THE PC
IS NOT INCREMENTED AND MADS IS NOT LOADED
BECAUSE IN THE LCK AND CCK ROUTINES THE SAME
ADDRESS WOULD BE CALLED

RT3A: USED FOR LC,SC,CW,CC

Figure 3.19.24b ADDRESSING ROUTINES RT2A THR. 7A

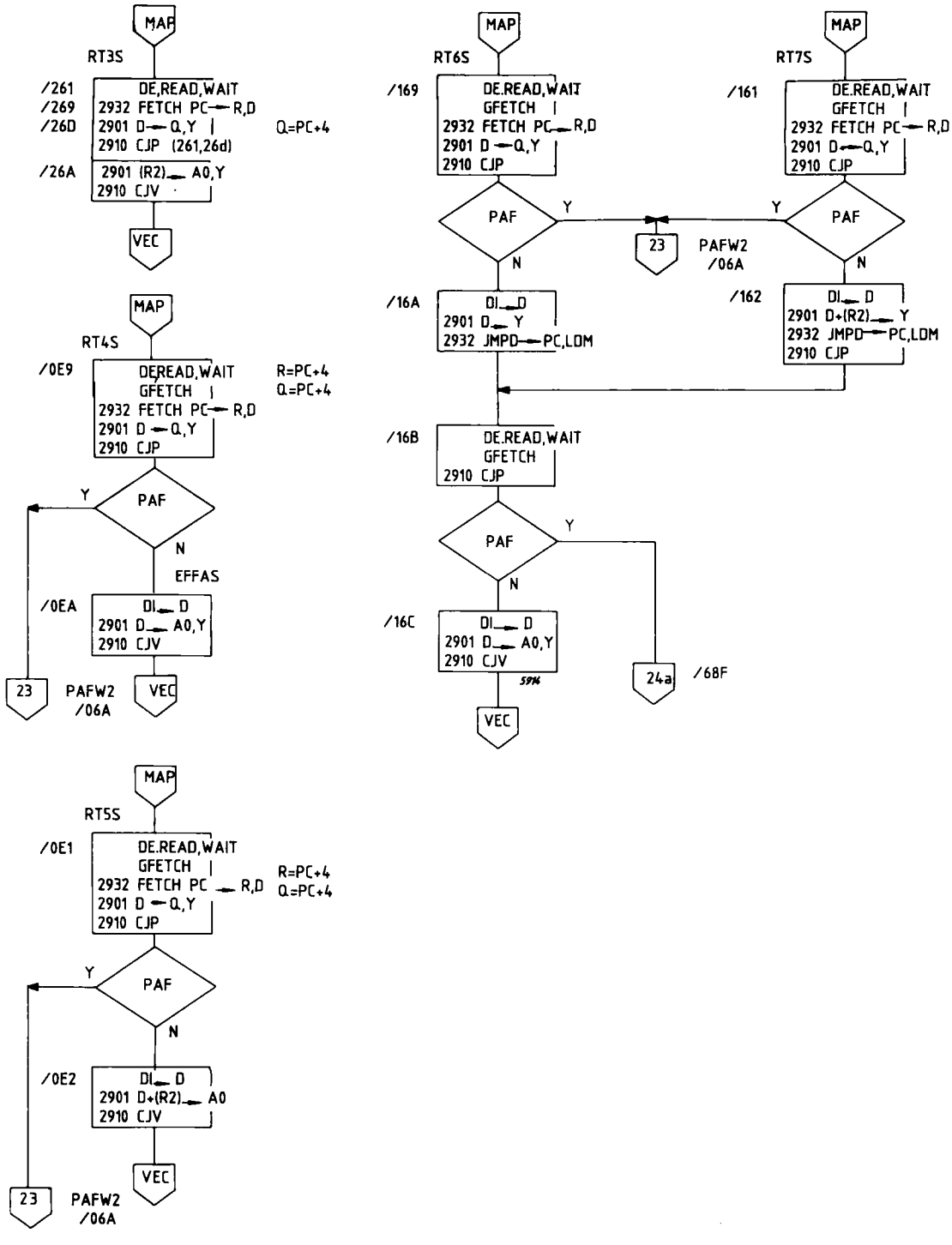


Figure 3.19.25 ADDRESSING ROUTINES RT3S THR. 7S

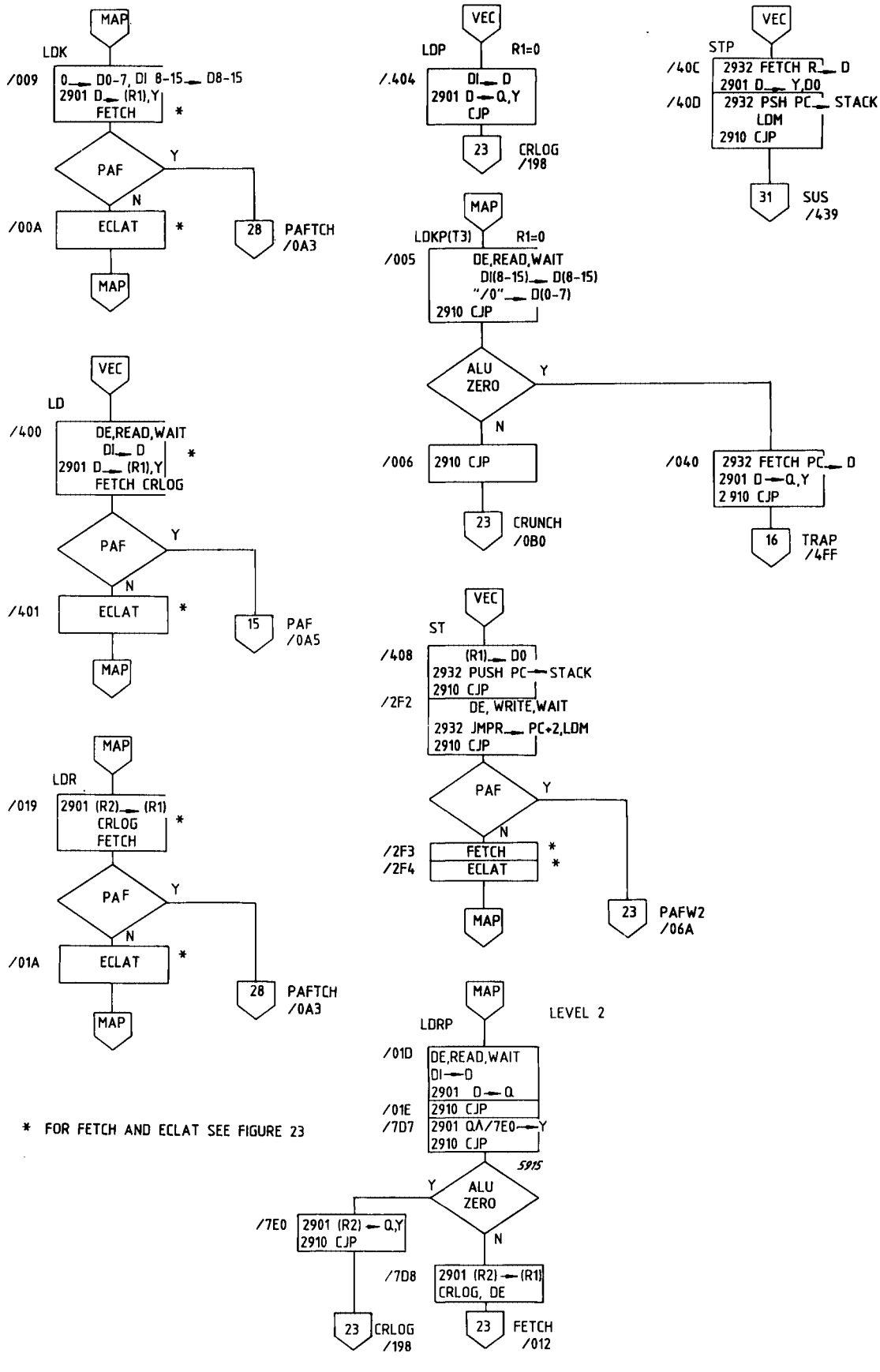


Figure 3.19.27 OPCODE 0: LDK, LDR, LDKP, LD, LDP, ST, STP

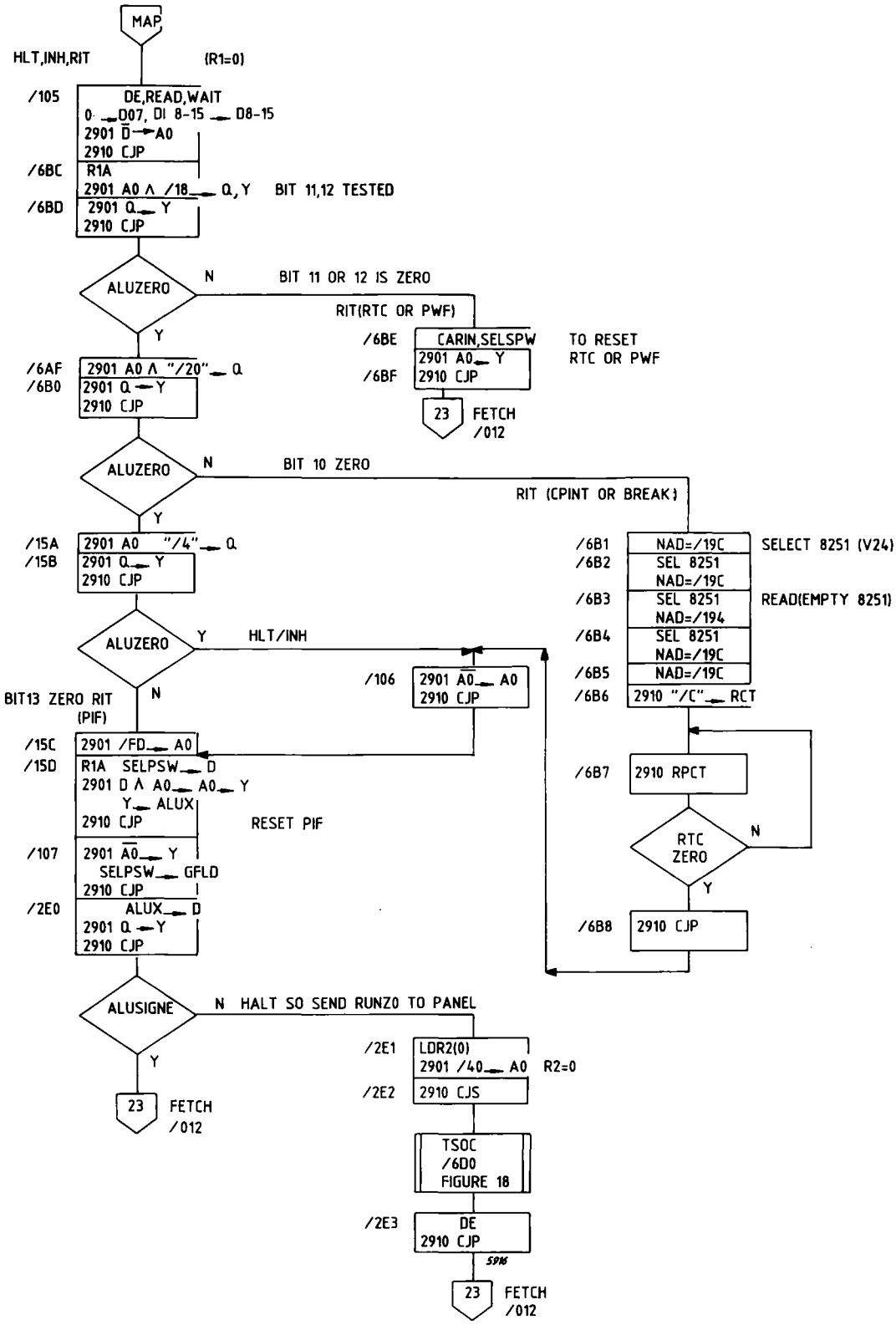


Figure 3.19.33 OPCODE 4: HLT, INH, RIT

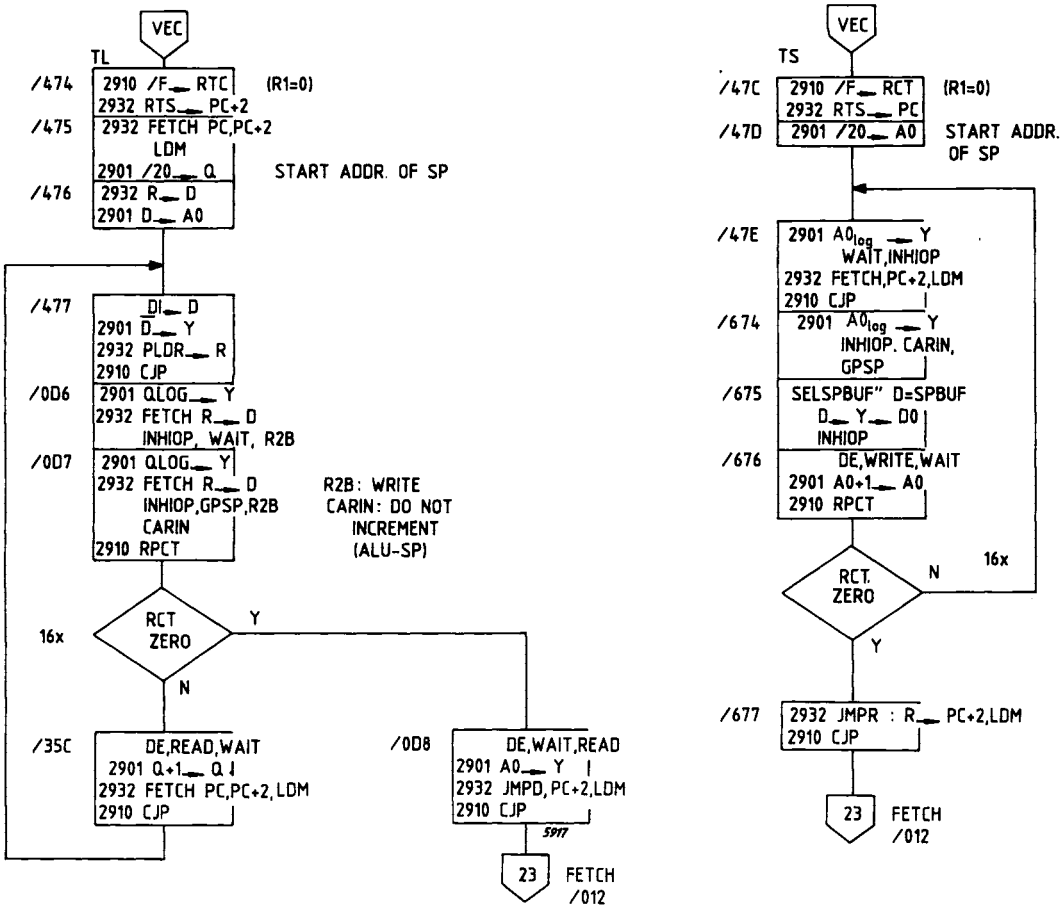
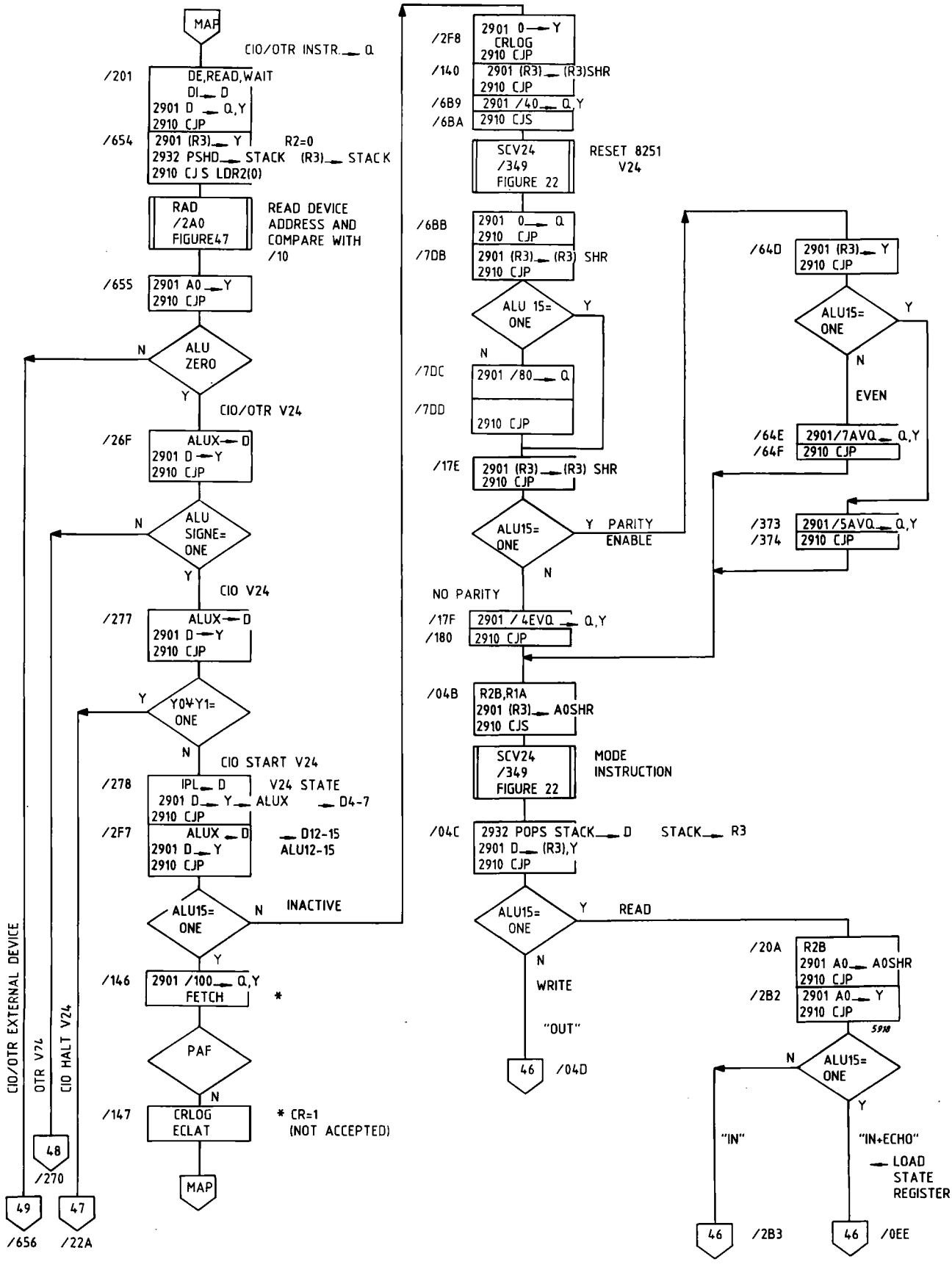


Figure 3.19.43 OPCODE 7: TL, TS



* FOR FETCH AND ECLAT SEE FIGURE 23

Figure 3.19.45 OPCODE 8: CIO/OTR

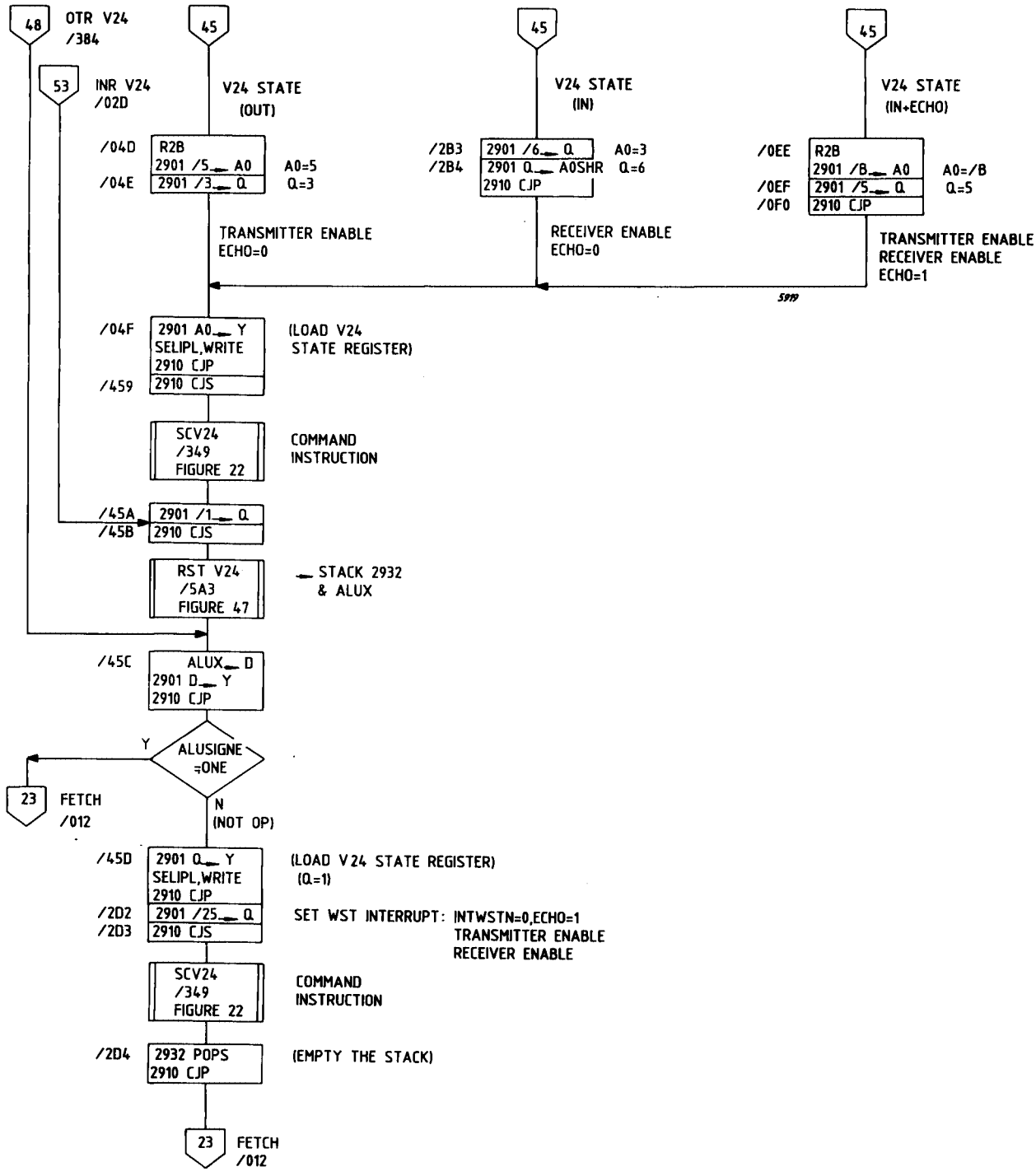


Figure 3.19.46 OPCODE 8: V24 STATES

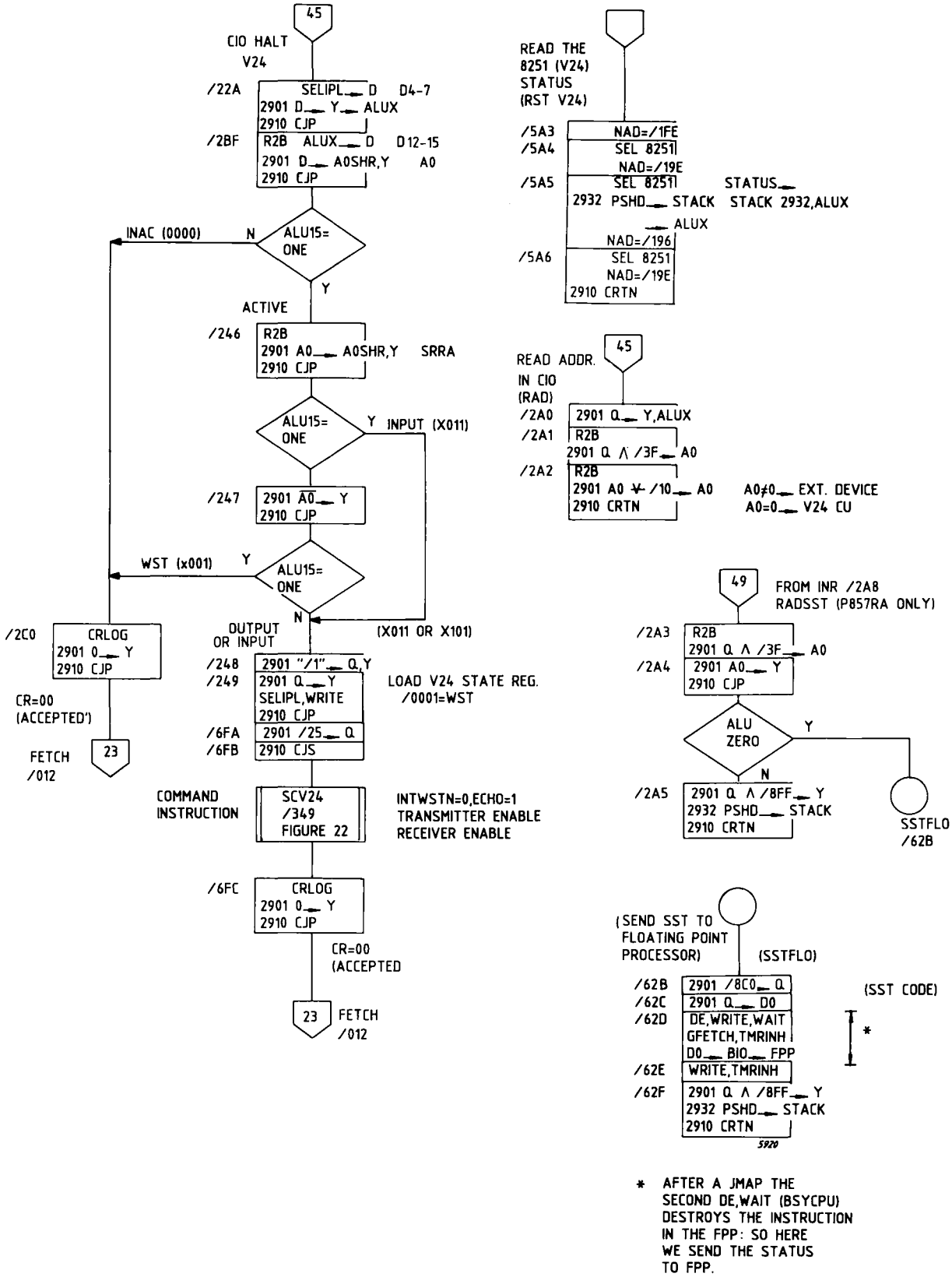


Figure 3.19.47 OPCODE 8: CIO HALT V24, RST V24, SSTFLO, RAD

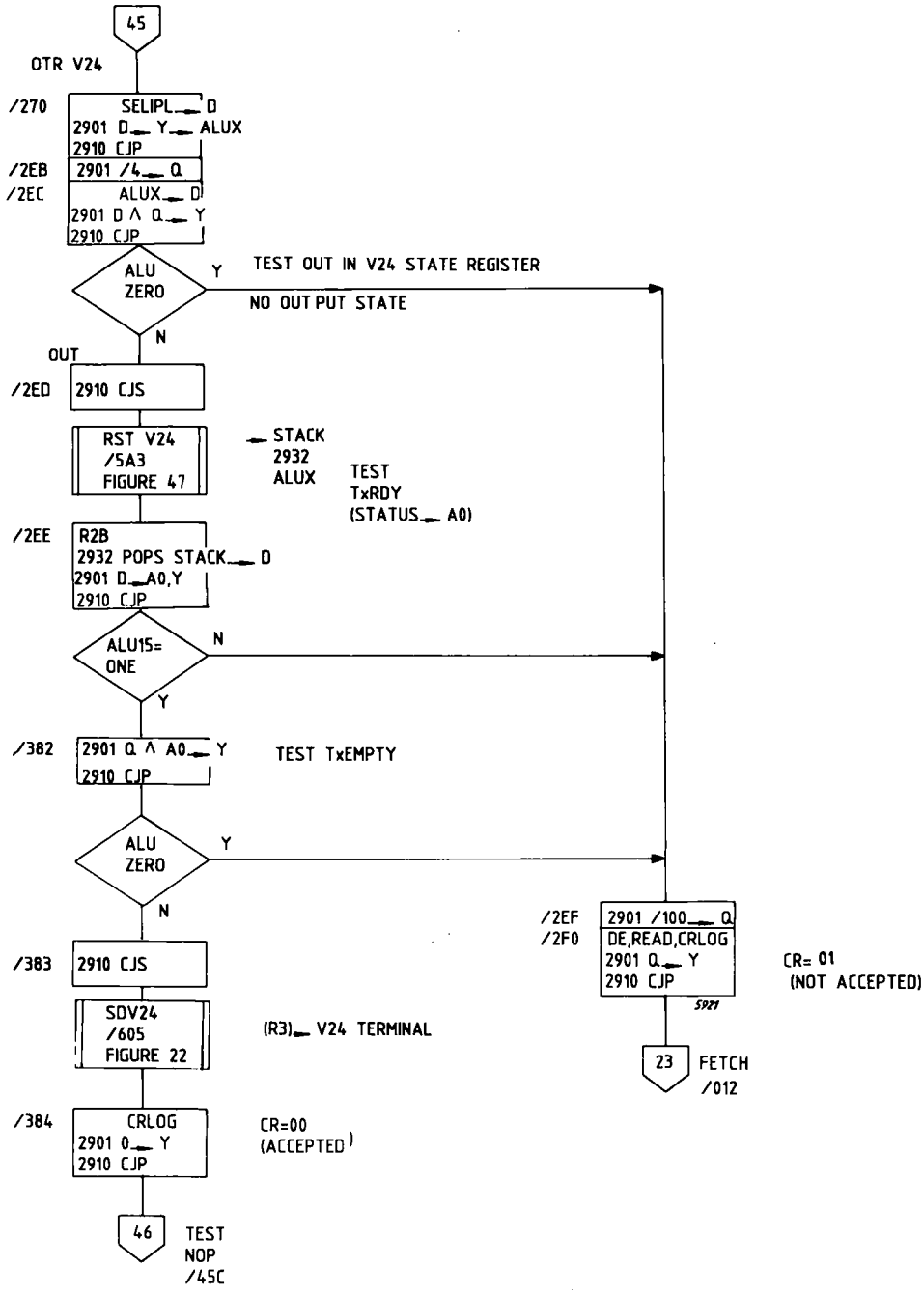


Figure 3.19.48 OPCODE 8: OTR-V24

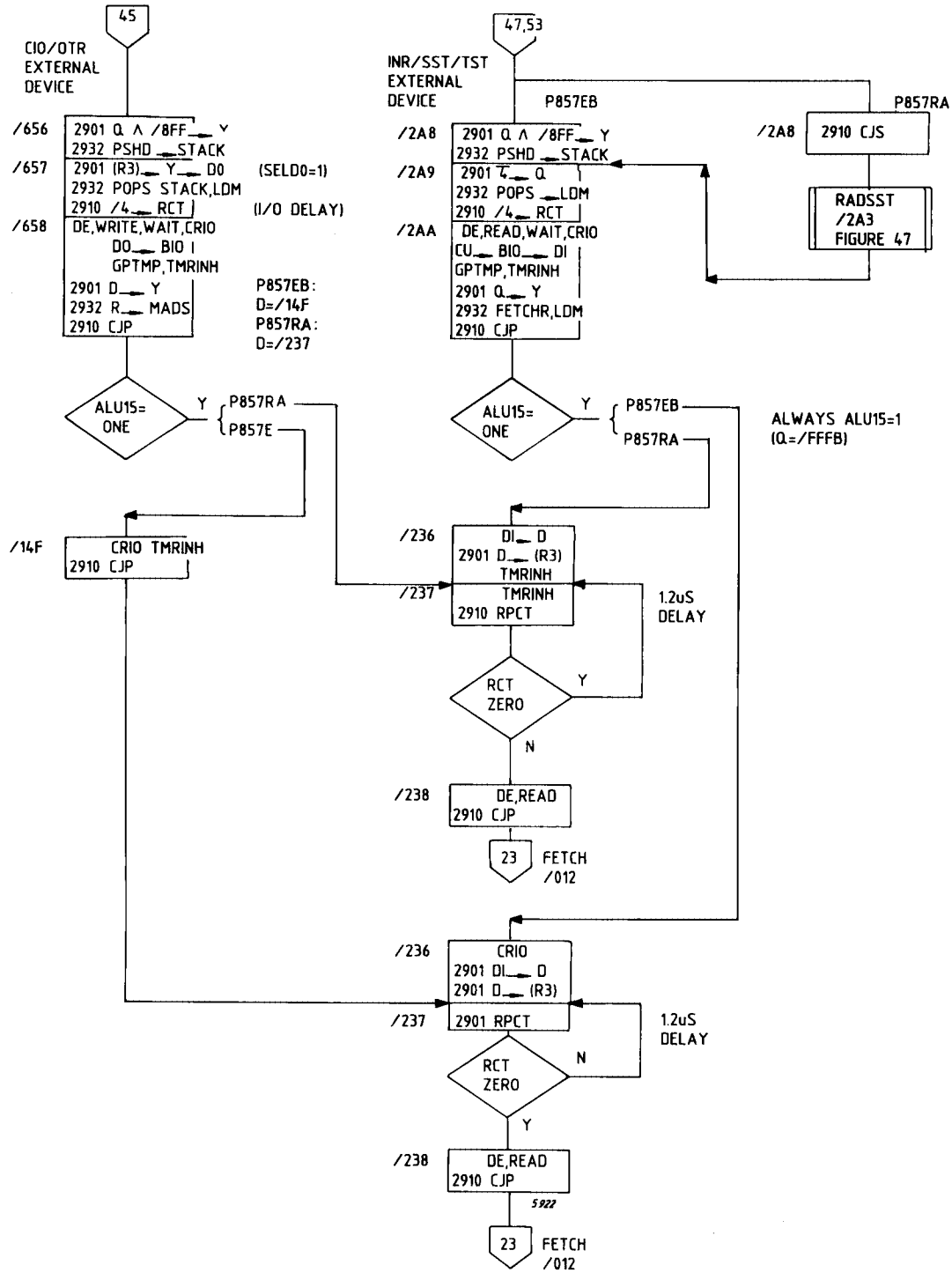
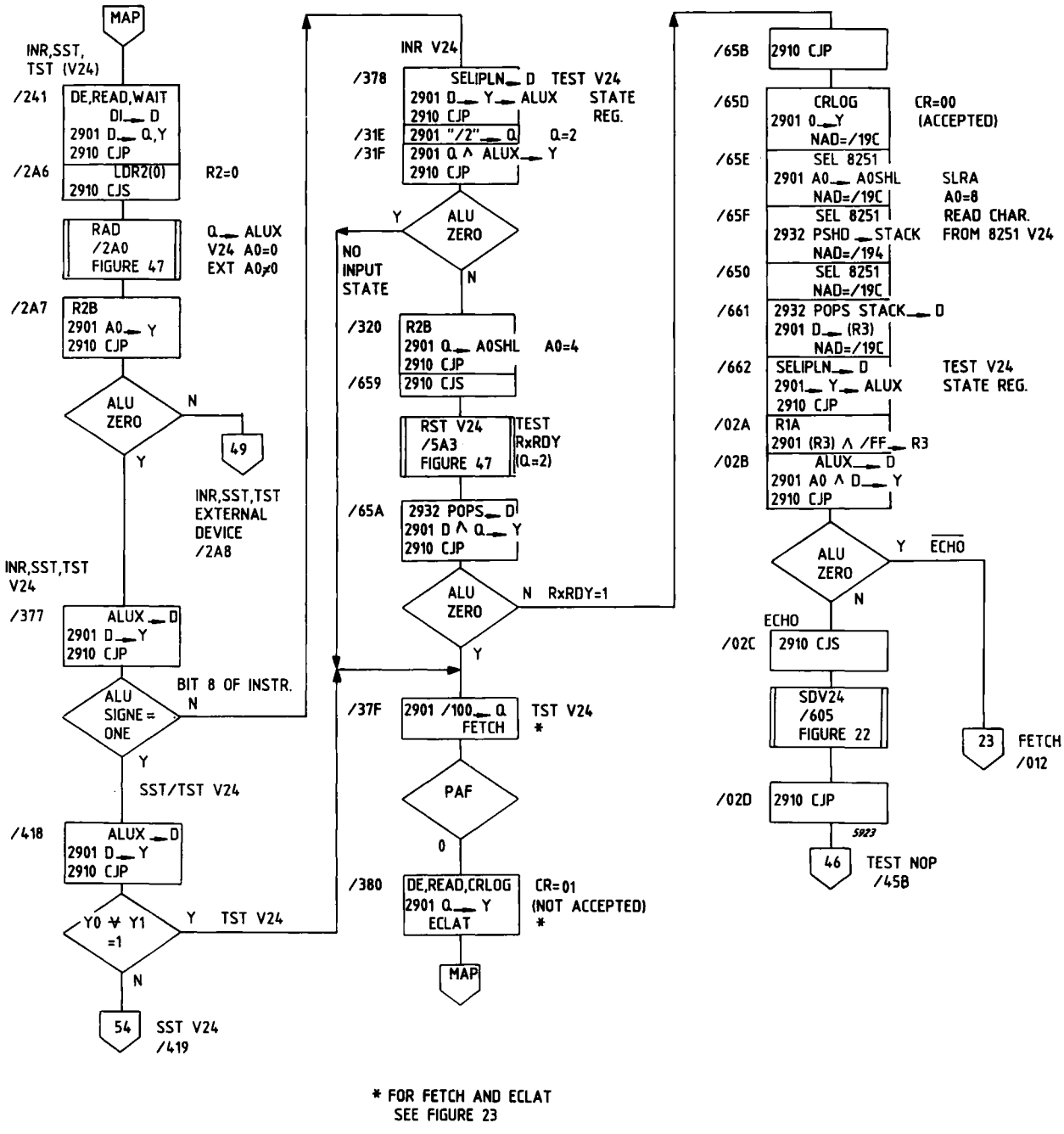


Figure 3.19.49 CIO/OTR EXTERNAL DEVICE INR/SST, TST EXTERNAL DEVICE



* FOR FETCH AND ECLAT
SEE FIGURE 23

Figure 3.19.53 OPCODE 9: INR, SST, TST (V24), INRV24, ECHO

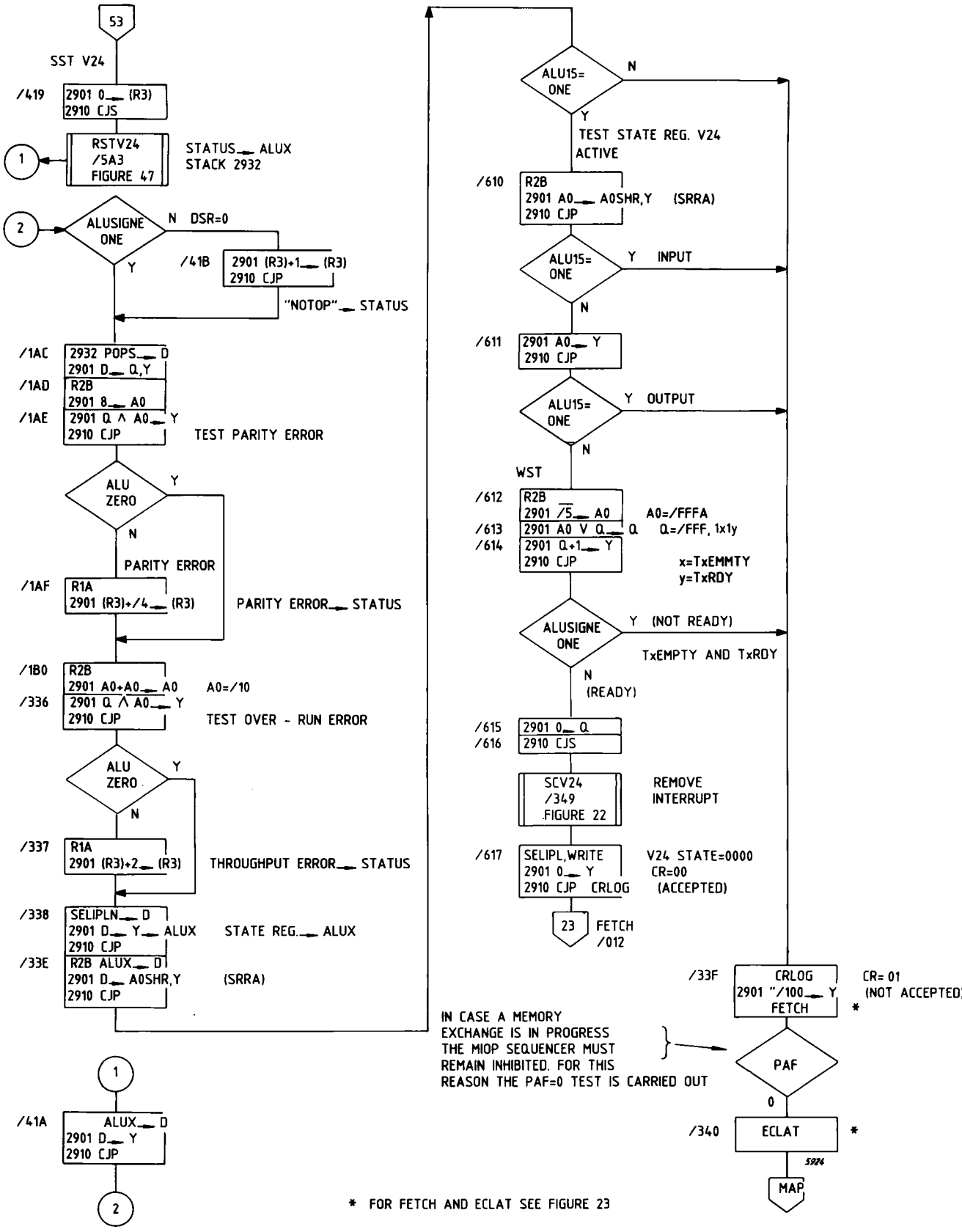


Figure 3.19.54 OPCODE 9: SSTV24

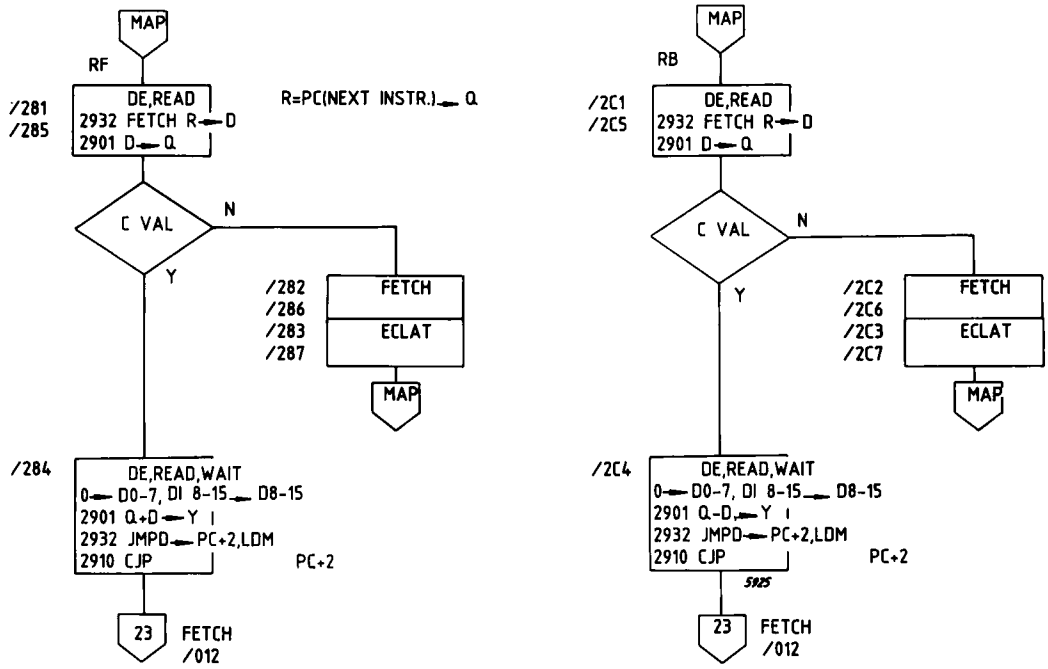


Figure 3.19.57 OPCODE 10: RF
OPCODE 11: RB

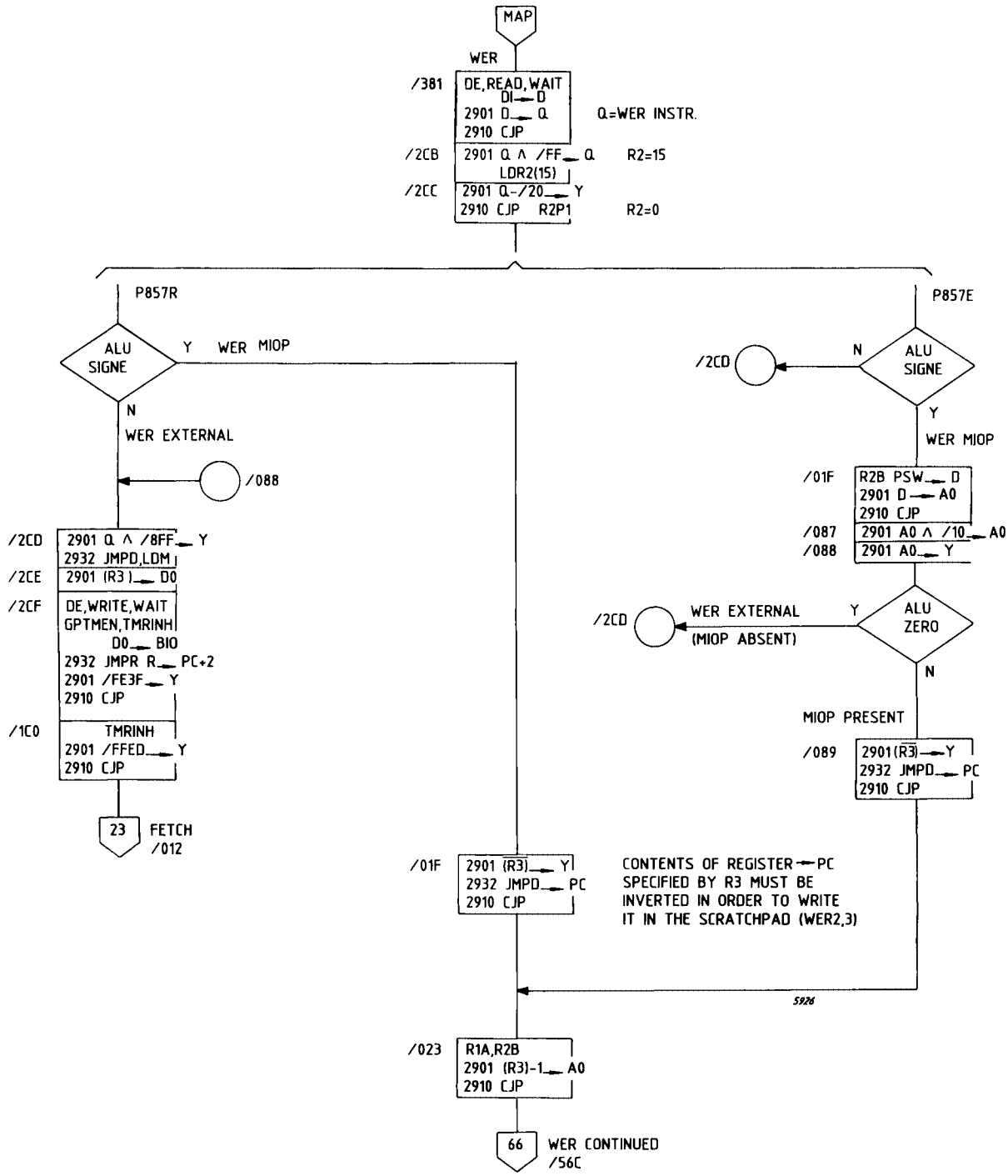
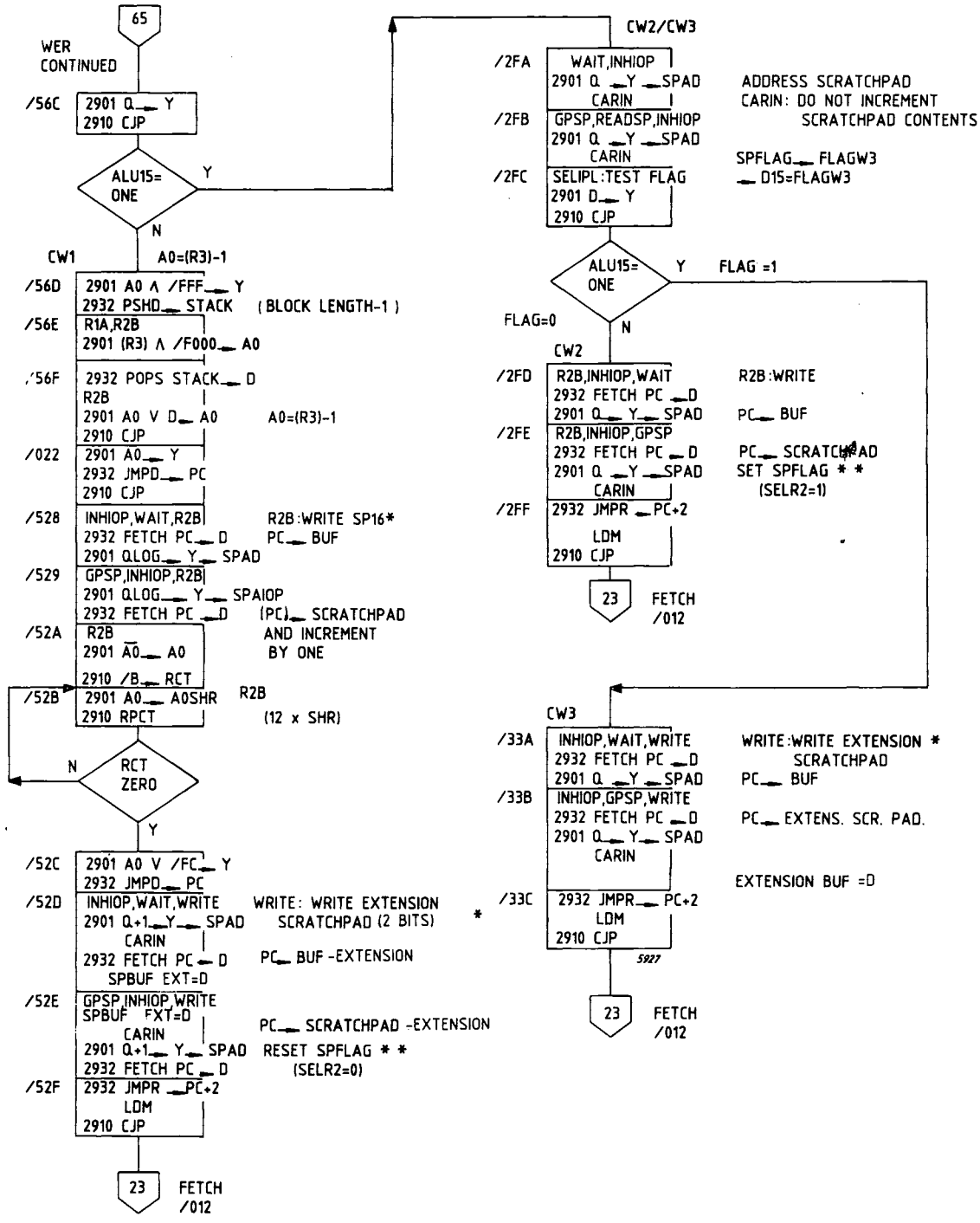


Figure 3.19.65 OPCODE 14: WER



* NOTE: SCRATCHPAD IS WRITTEN INVERTEDLY

* * NOTE: R2B=SELR2=1 MEANS WRITE SCRATCHPAD AND SET SPFLAG
SELR2=0 MEANS RESET SPFLAG

Figure 3.19.66 OPCODE 14: WER (CONT'D)

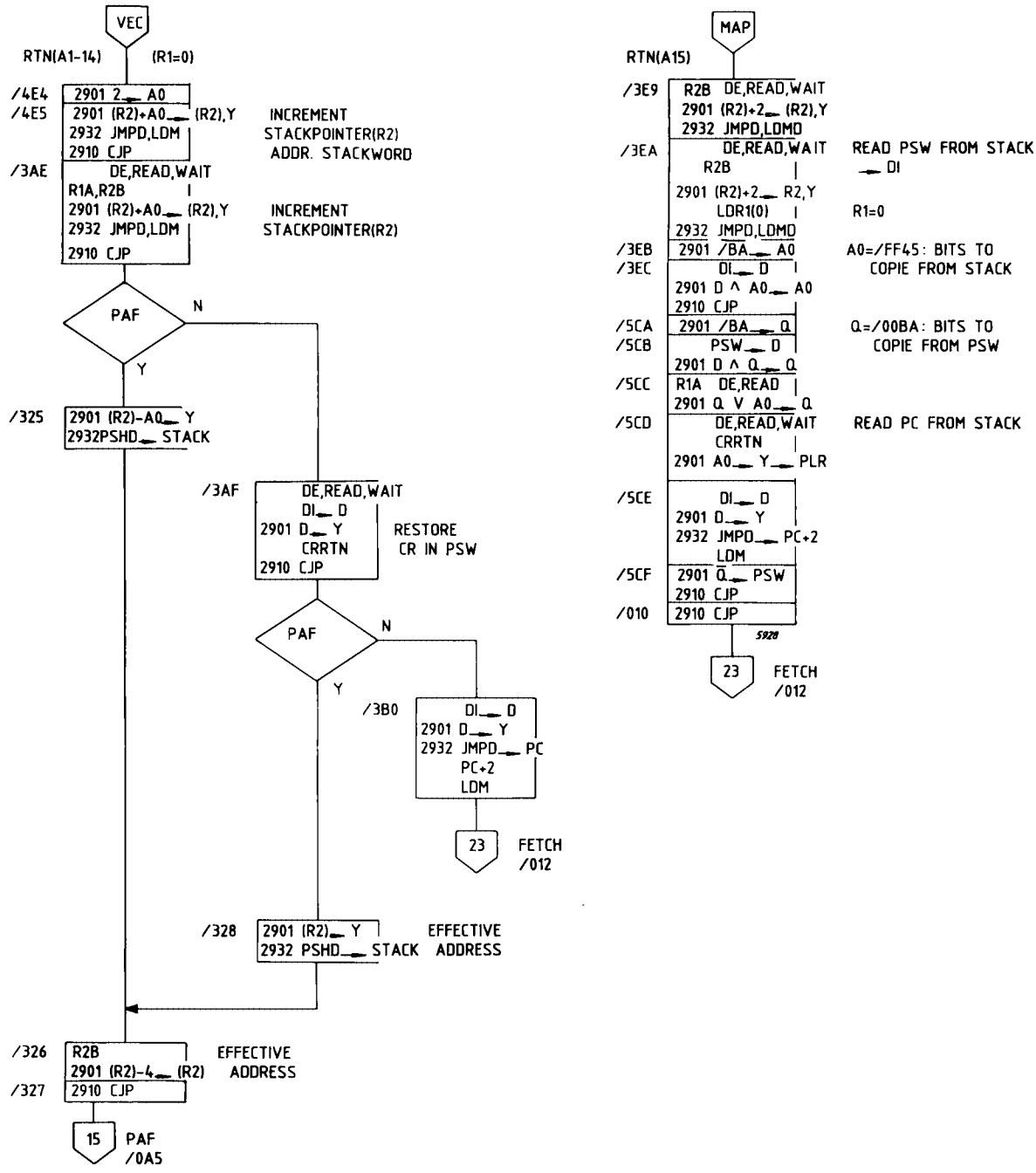
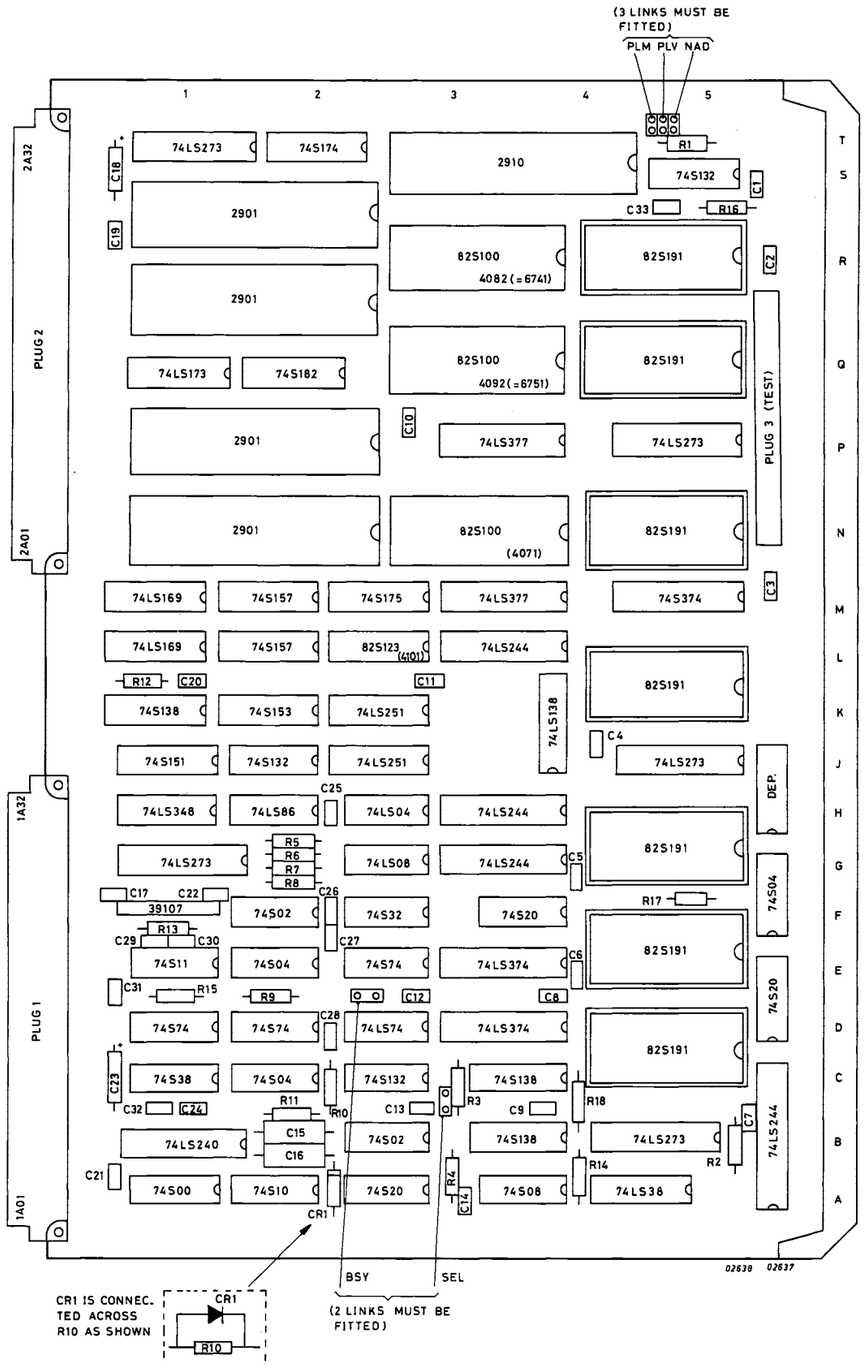


Figure 3.19.70 OPCODE 14: RTN, (A1-A15)

LIST OF ILLUSTRATIONS


(3 LINKS MUST BE FITTED)
PLM PLV NAD
1
2
3
4
5
2A32
PLUG 2
2A01
1A32
PLUG 1
1A01
74LS273
74S174
2910
R1
74S132
C1
C33
R16
C18
C19
2901
82S100
4082 (=6741)
82S191
C2
2901
82S100
4092 (=6751)
82S191
74LS173
74S182
PLUG 3 (TEST)
C10
2901
74LS377
74LS273
2901
82S100
(4071)
82S191
74LS169
74S157
74S175
74LS377
74S374
C3
74LS169
74S157
82S123
(4101)
74LS244
82S191
R12
C20
C11
74S138
74S153
74LS251
74LS138
C4
74S151
74S132
74LS251
74LS273
DEP.
74LS348
74LS86
C25
74LS04
74LS244
82S191
74LS273
R5
R6
R7
R8
74LS08
74LS244
C5
74S04
C17
C22
39107
C26
74S02
74S32
74S20
R17
82S191
R13
C29
C30
C27
74S11
74S04
74S74
74LS374
C6
74S20
C31
R15
R9
C12
C8
74S74
74S74
C28
74LS74
74LS374
82S191
C23
74S38
74S04
74S132
74S138
C32
C24
R11
R10
C13
R3
C9
R18
C7
74LS244
74LS240
C15
C16
74S02
74S138
74LS273
R2
C21
R14
74S00
74S10
74S20
R4
C14
74S08
74LS38
CR1
A
B
C
D
E
F
G
H
J
K
L
M
N
P
Q
R
S
T
02638
02637
BSY
SEL
(2 LINKS MUST BE FITTED)
CR1 IS CONNEC. TED ACROSS R10 AS SHOWN
CR1
R10

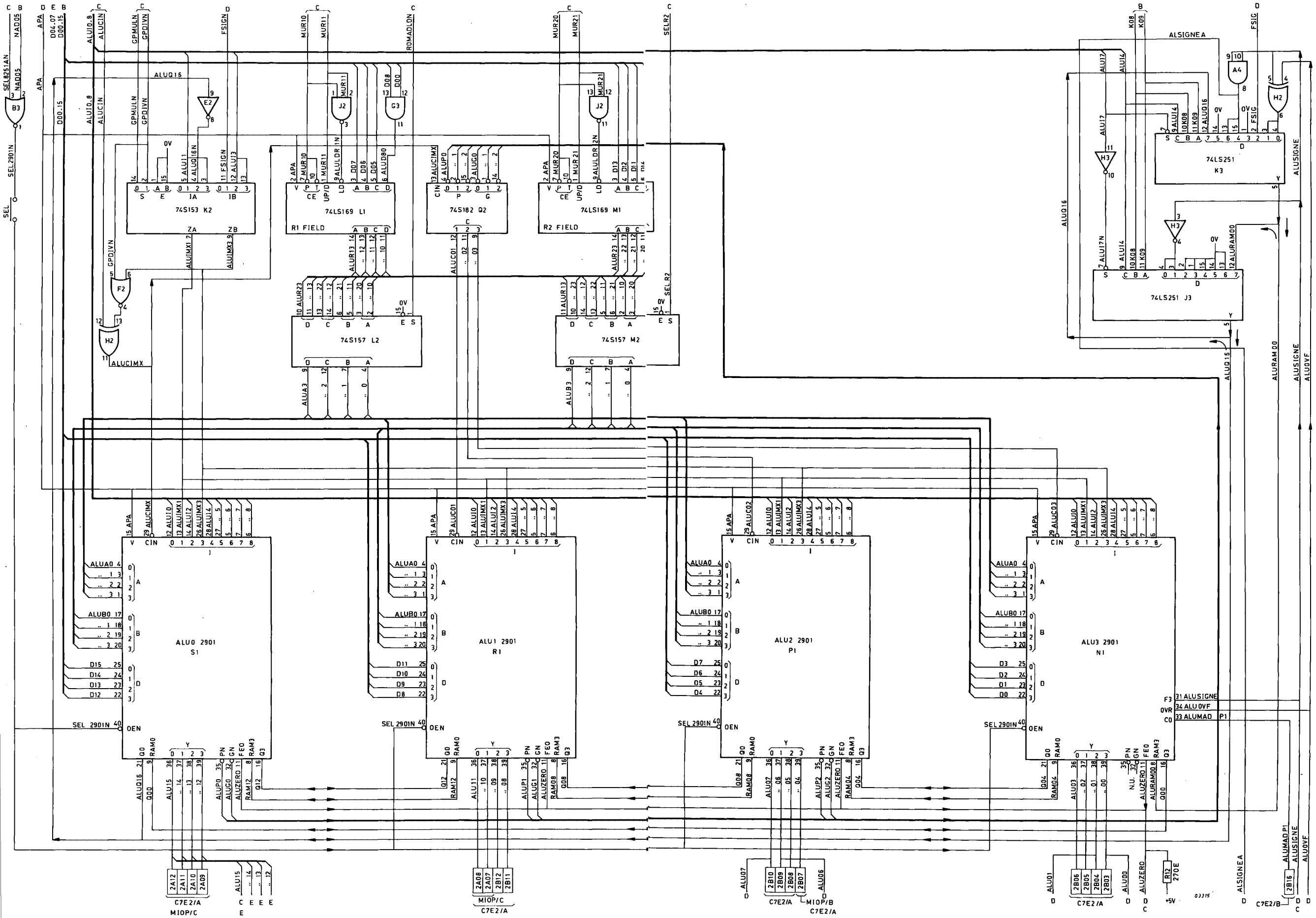


Figure 4.1A (C7E1B) ARITHMETIC LOGIC UNITS

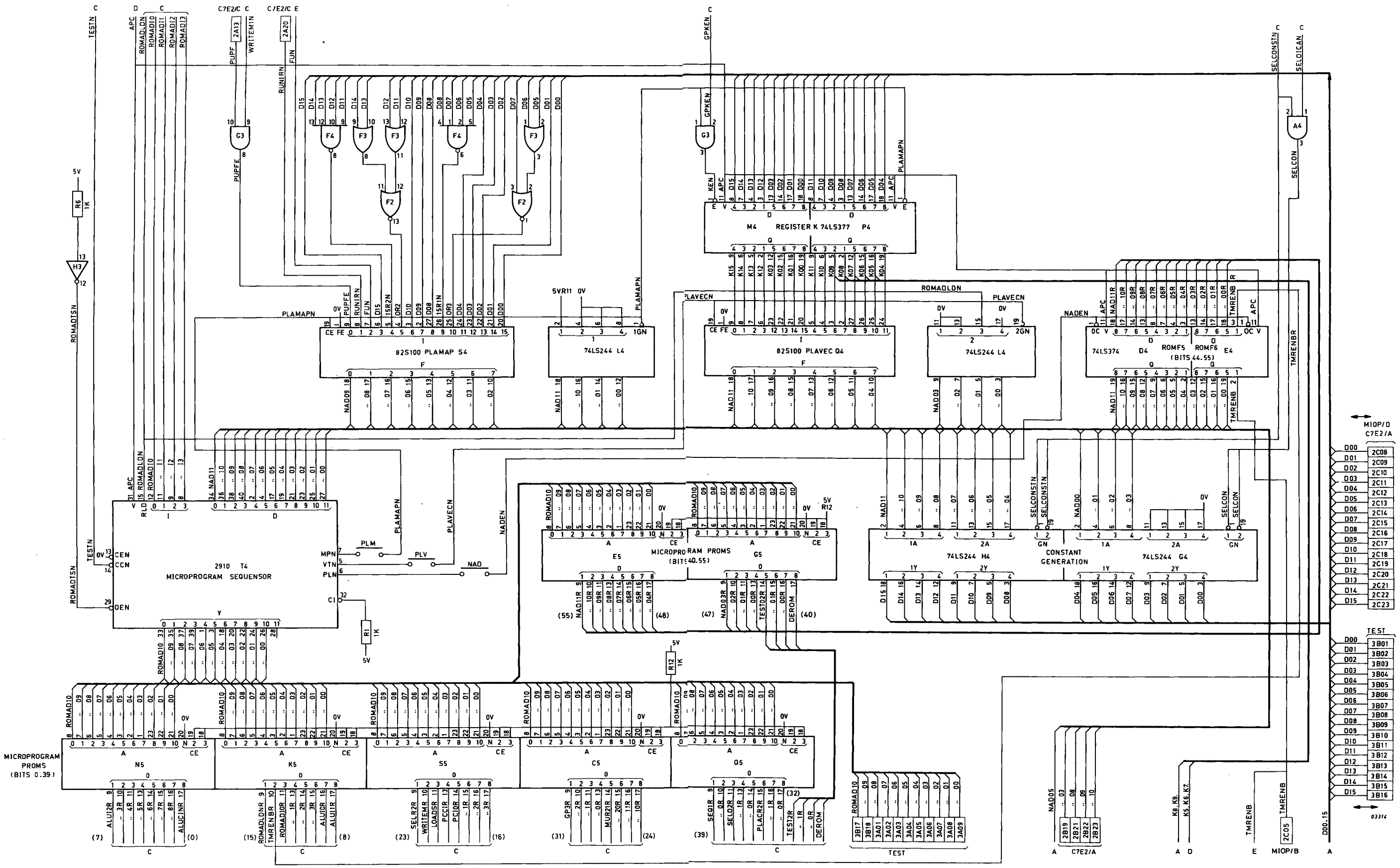


Figure 4.1B (C7E1A) MICRO PROGRAM

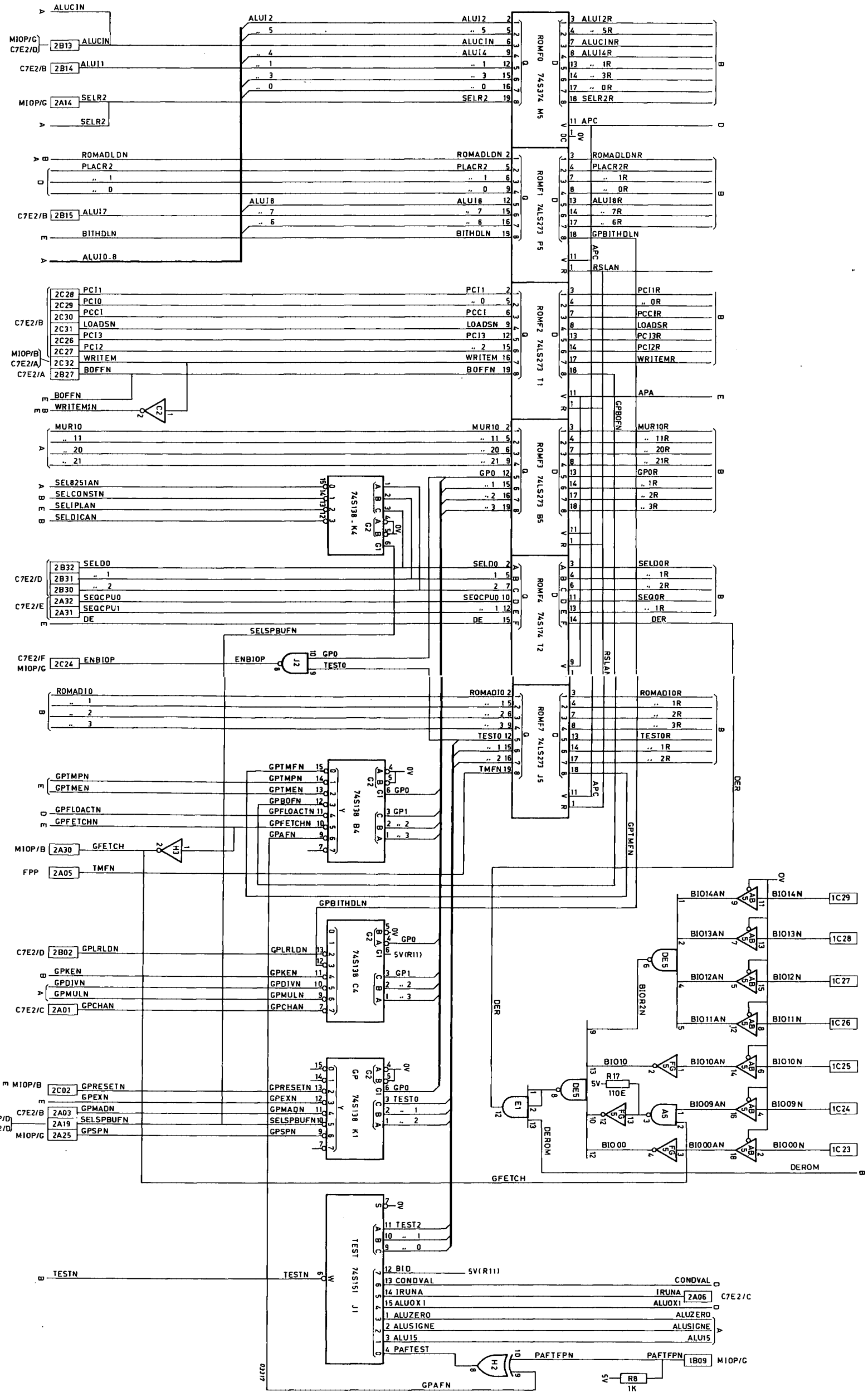
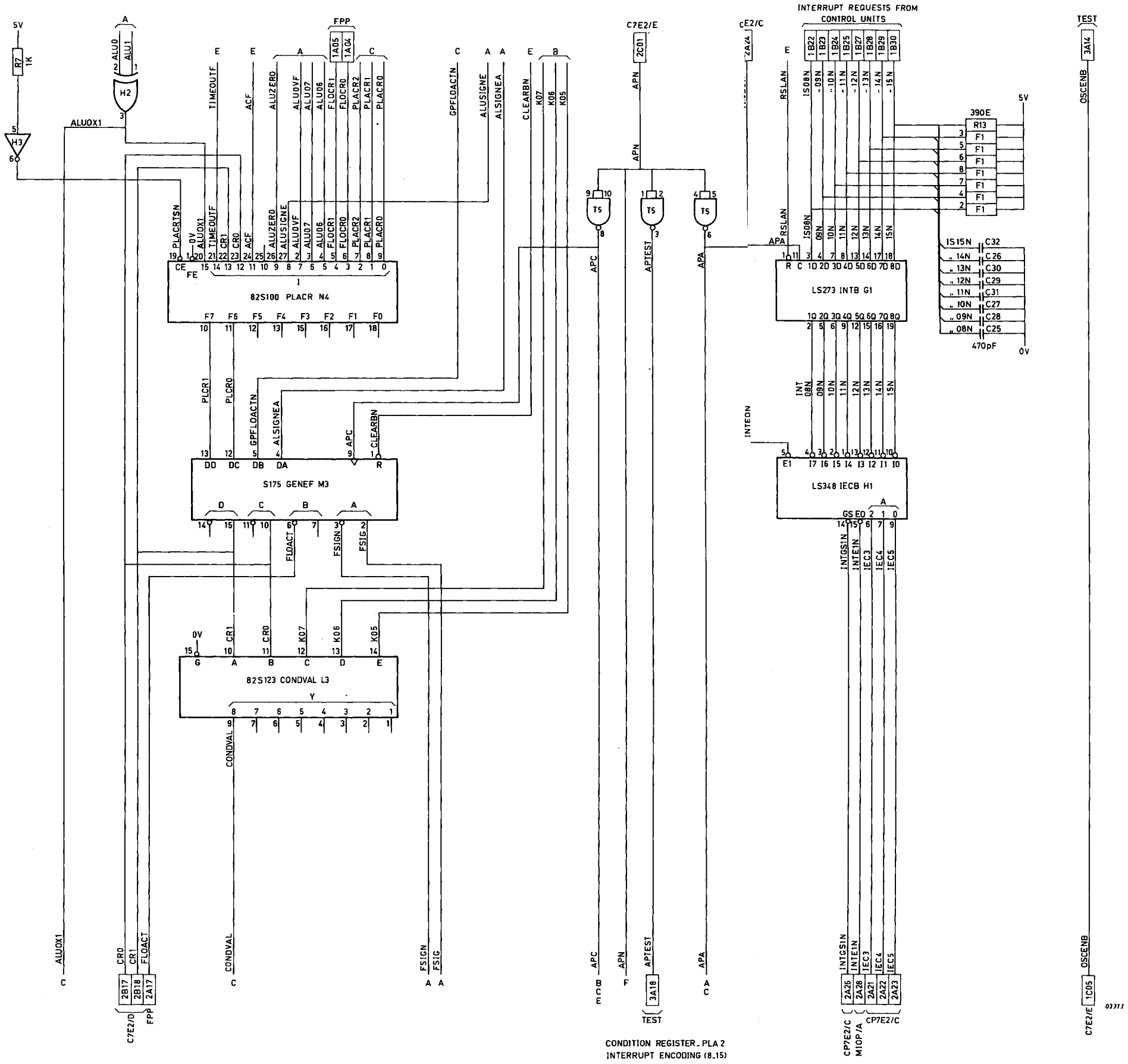


Figure 4.1C (C7E1B) MICRO PROGRAM REGISTER



CONDITION REGISTER_PLA 2
INTERRUPT ENCODING (8_15)

Figure 4.1D (C7E1B) CONDITION REGISTER INTERRUPT ENCODING (8-15)

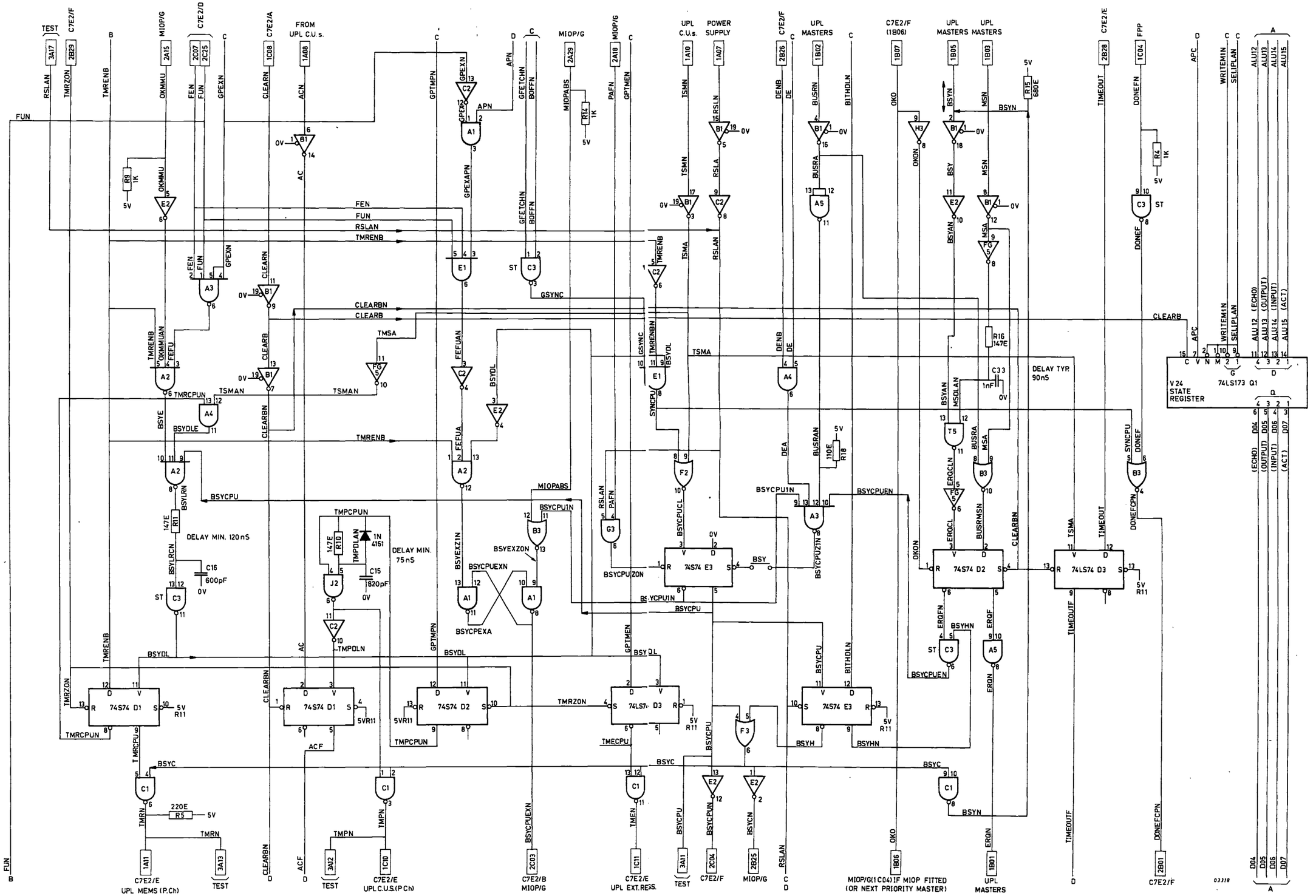
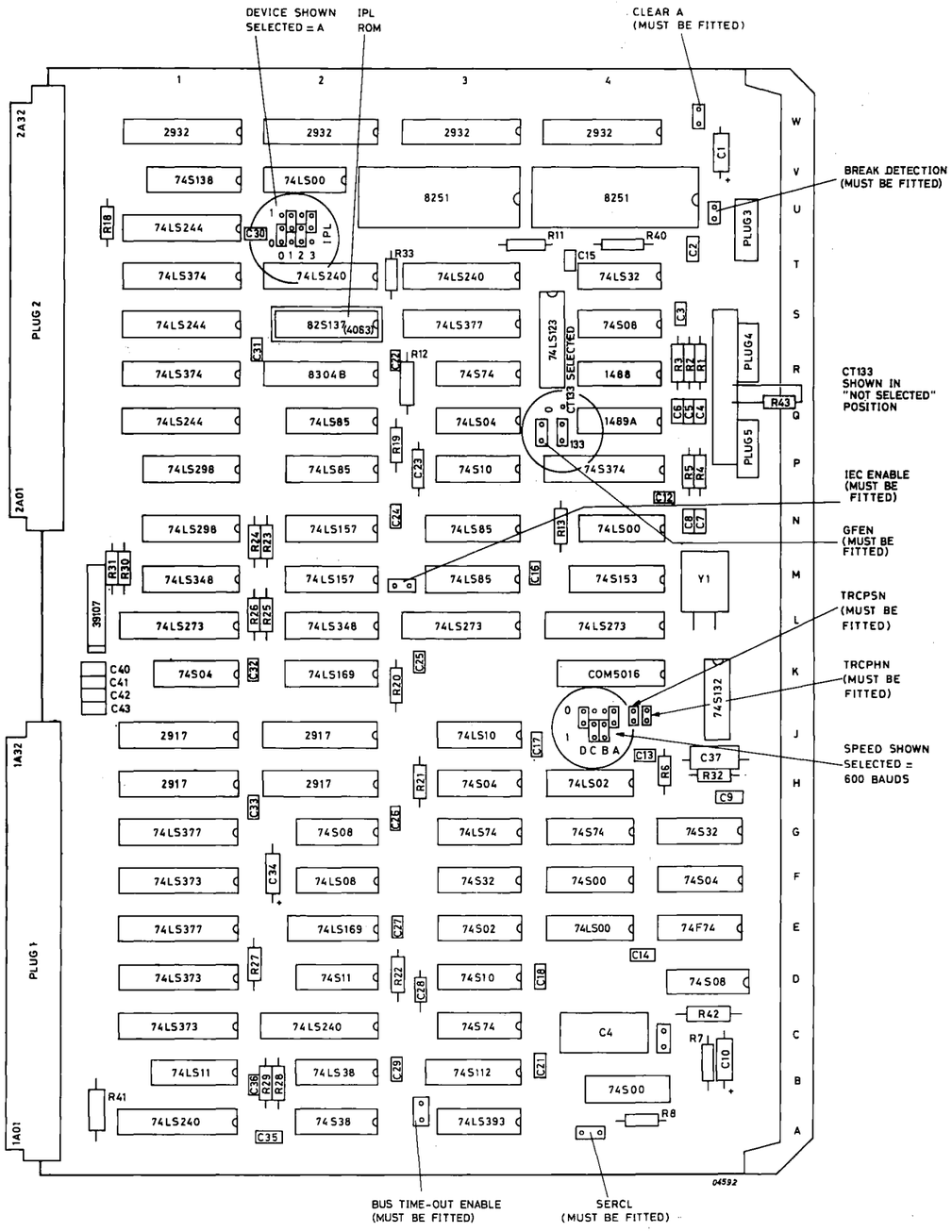


Figure 4.1E (C7E1B) BUS CONTROL LOGIC
V24 STATE REGISTER


DEVICE SHOWN SELECTED = A
IPL ROM
CLEAR A (MUST BE FITTED)
BREAK DETECTION (MUST BE FITTED)
CT133 SHOWN IN "NOT SELECTED" POSITION
IEC ENABLE (MUST BE FITTED)
GFEN (MUST BE FITTED)
TRCPSN (MUST BE FITTED)
TRCPHN (MUST BE FITTED)
SPEED SHOWN SELECTED = 600 BAUDS
BUS TIME-OUT ENABLE (MUST BE FITTED)
SERCL (MUST BE FITTED)
PLUG 1
PLUG 2
2A32
2A01
1A32
1A01
2932
74S138
74LS00
8251
74LS244
74LS374
74LS240
74LS32
82S137
74063
74LS377
74S08
74LS123
74S74
1488
8304B
74LS85
74LS04
1489A
74S10
74S374
74LS157
74LS153
74LS348
74LS273
74LS169
COM5016
74S132
2917
74LS10
74S04
74LS02
74S32
74S00
74F74
74S11
74LS38
74S112
74LS393
74S38
74LS240
C4
Y1
IPL
DCBA
04592

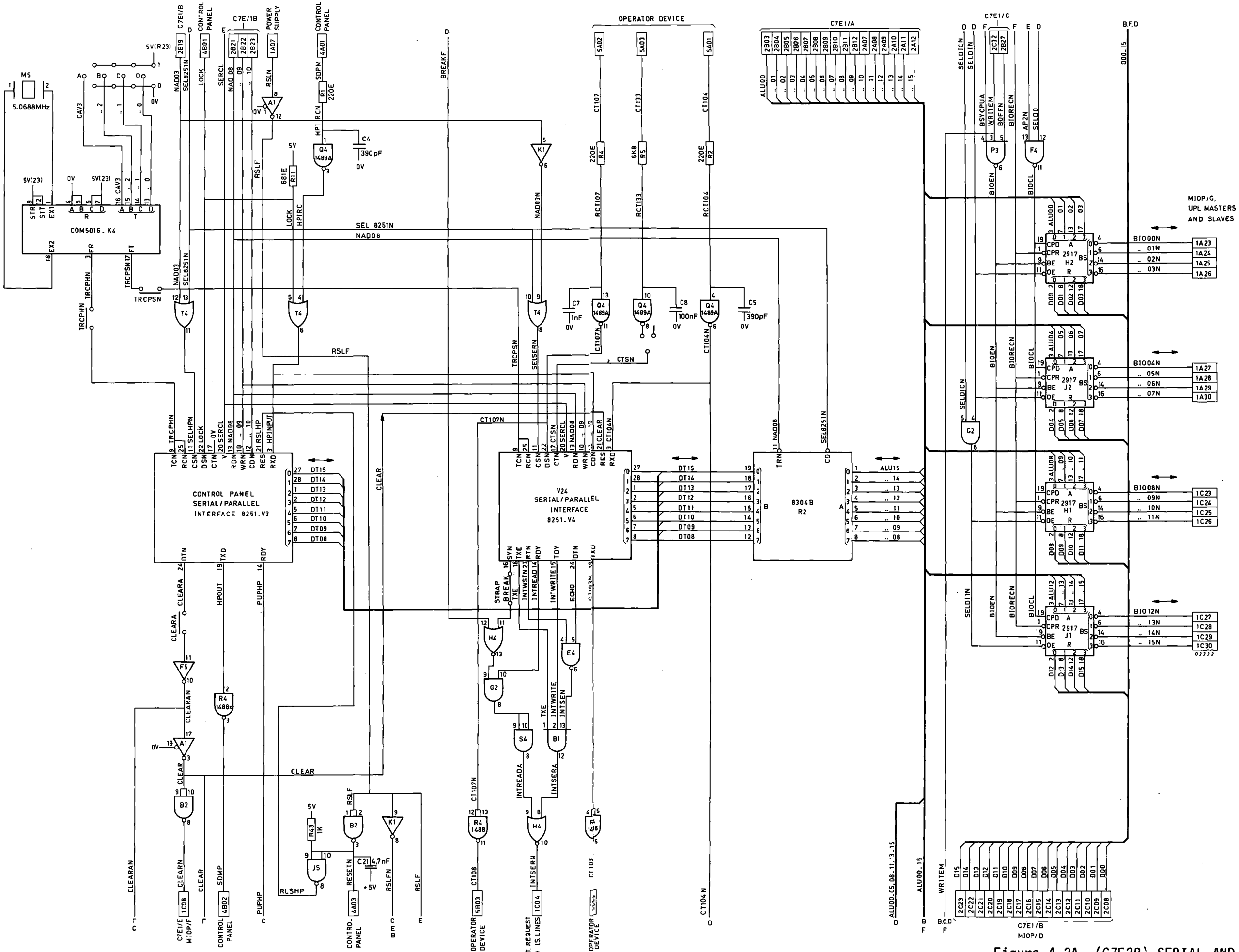


Figure 4.2A (C7E2B) SERIAL AND PARALLEL INTERFACE

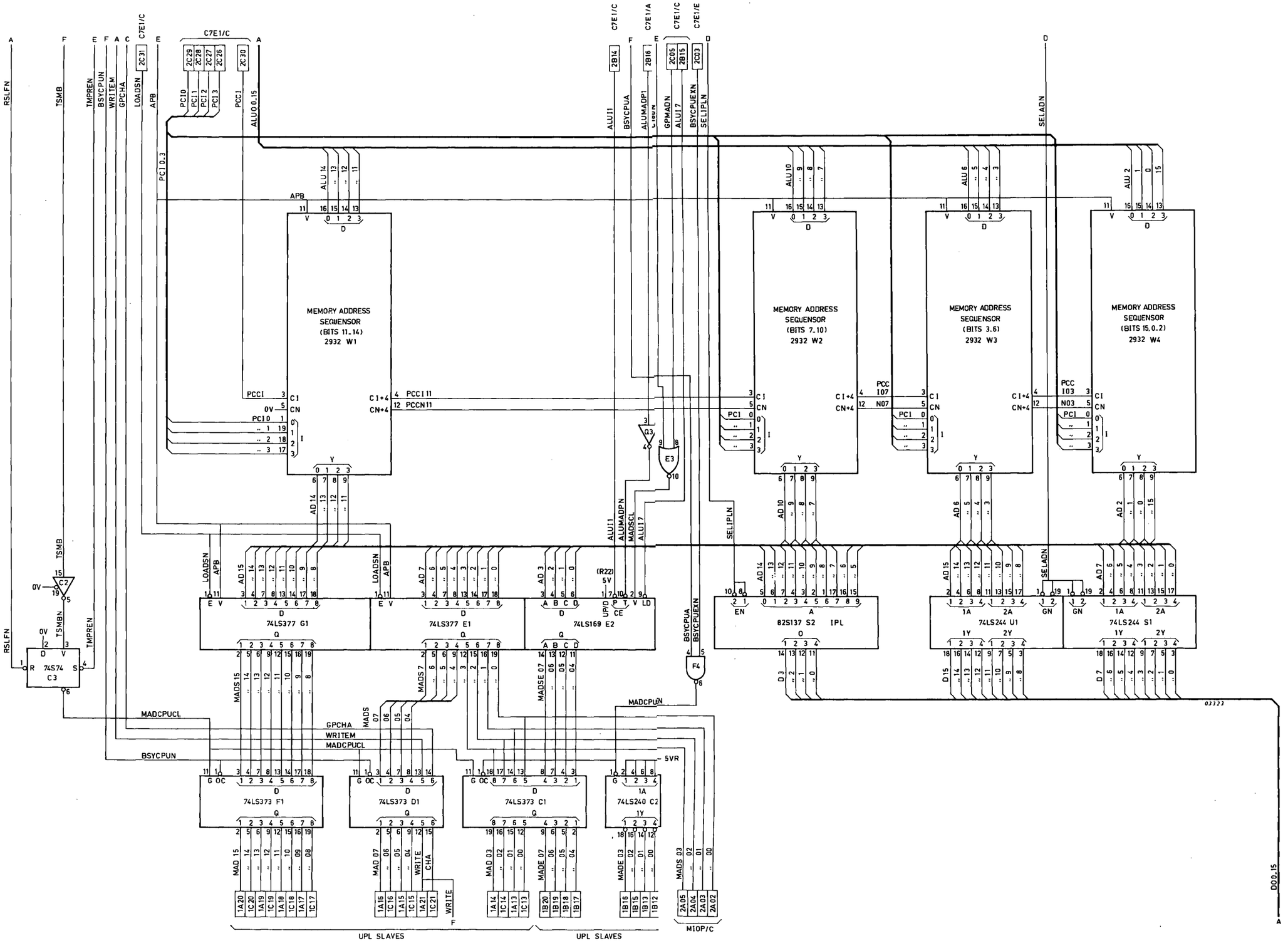


Figure 4.2B (C7E2B) MEMORY ADDRESSING, IPL

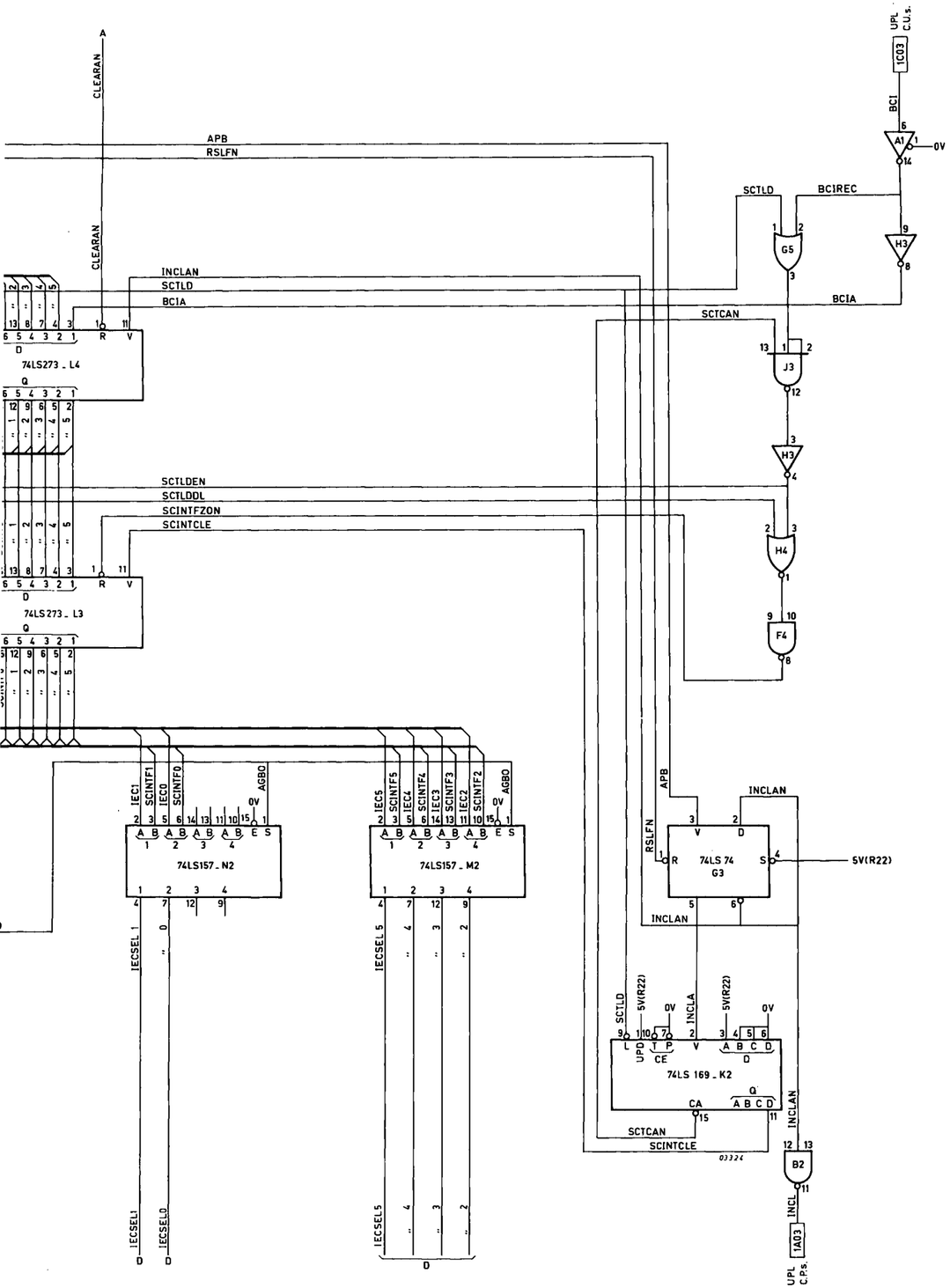
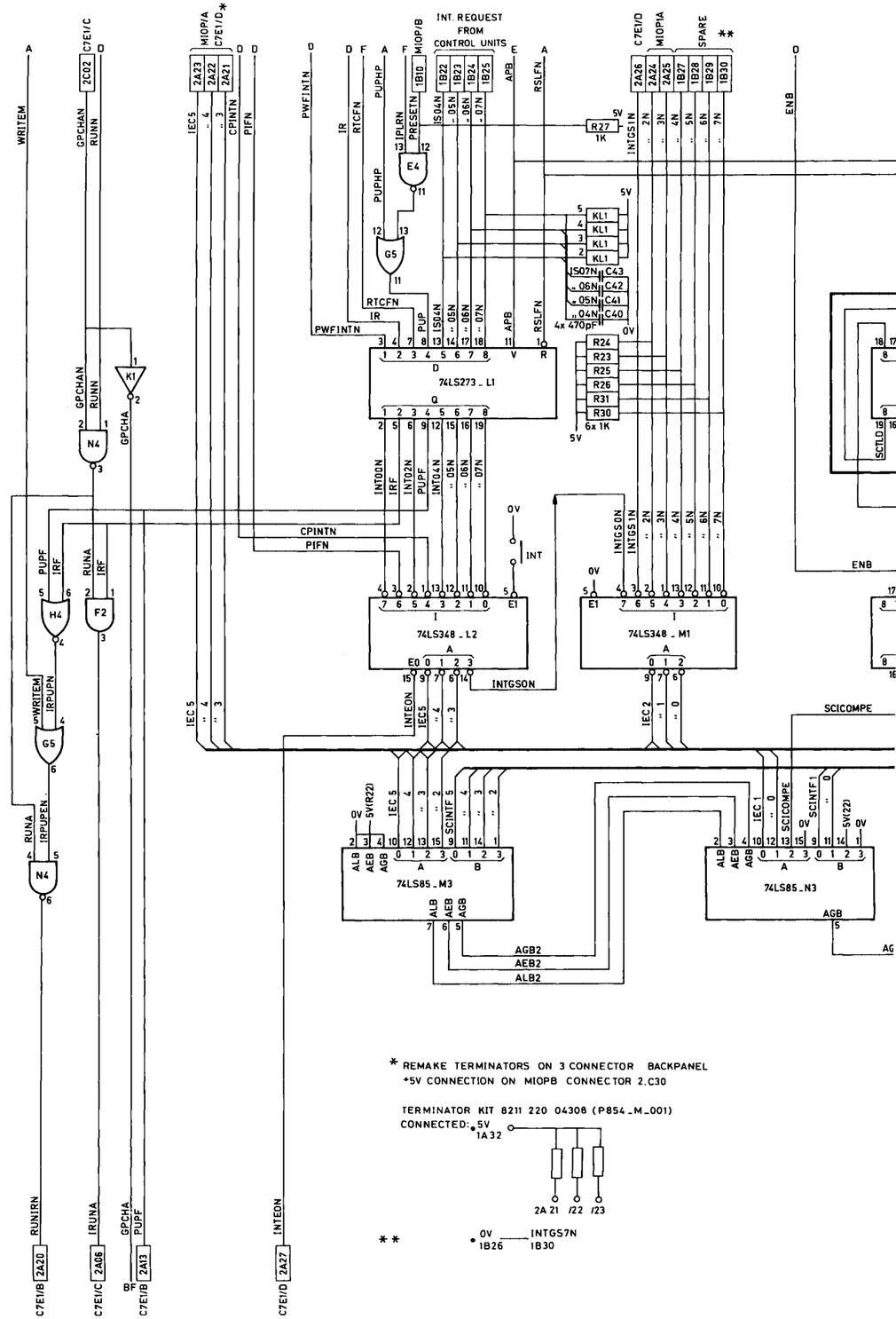


Figure 4.2C (C7E2B) INTERRUPTS, PARALLEL/ SERIAL ENCODING SERIAL CLOCK



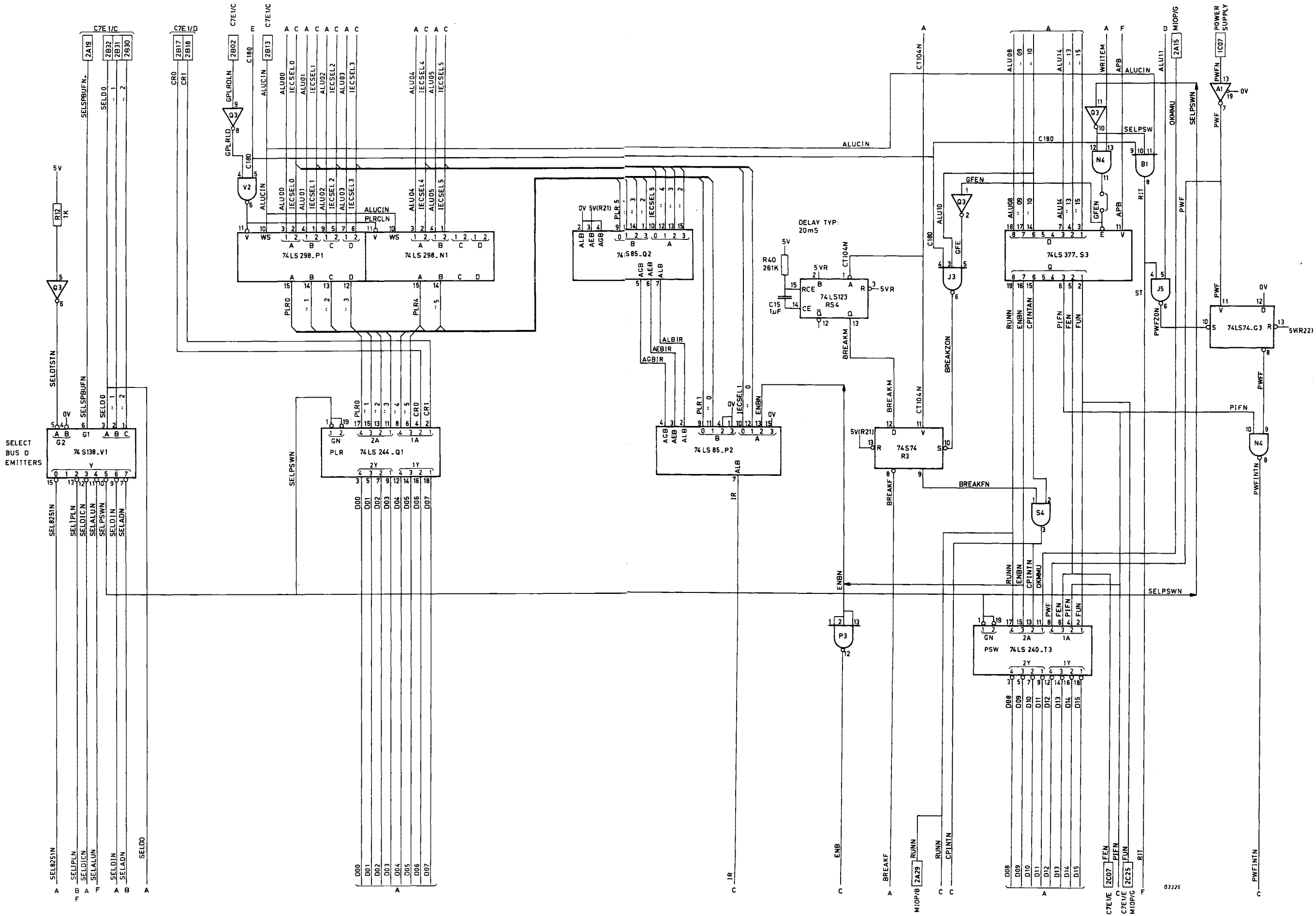


Figure 4.2D (C7E2B) SELECT D-BUS (DECODE) INTERRUPT LOGIC, PROGRAM STATUS WORD

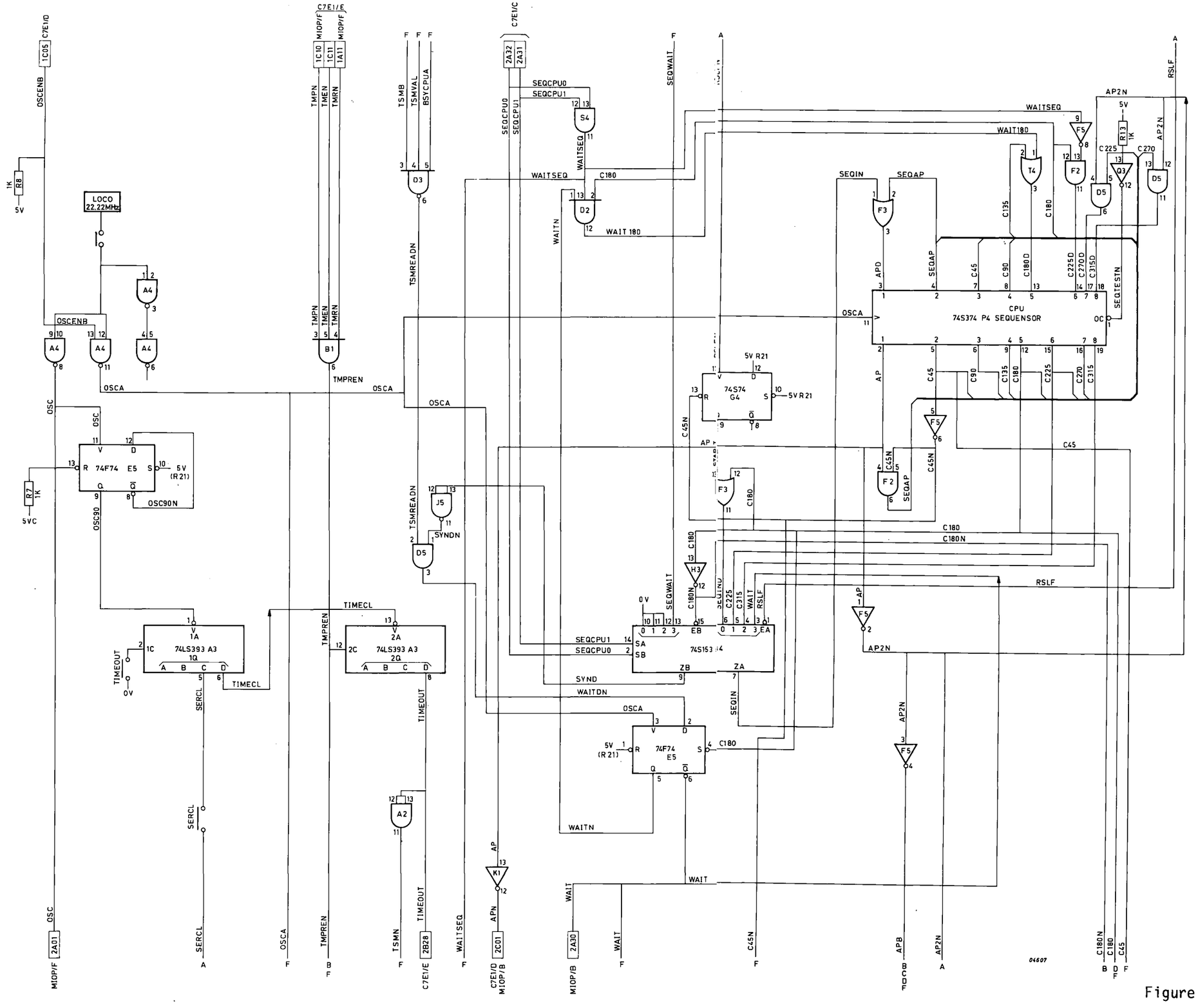


Figure 4.2E (C7E2B) SYSTEM CLOCK CPU SEQUENSOR TIME OUT

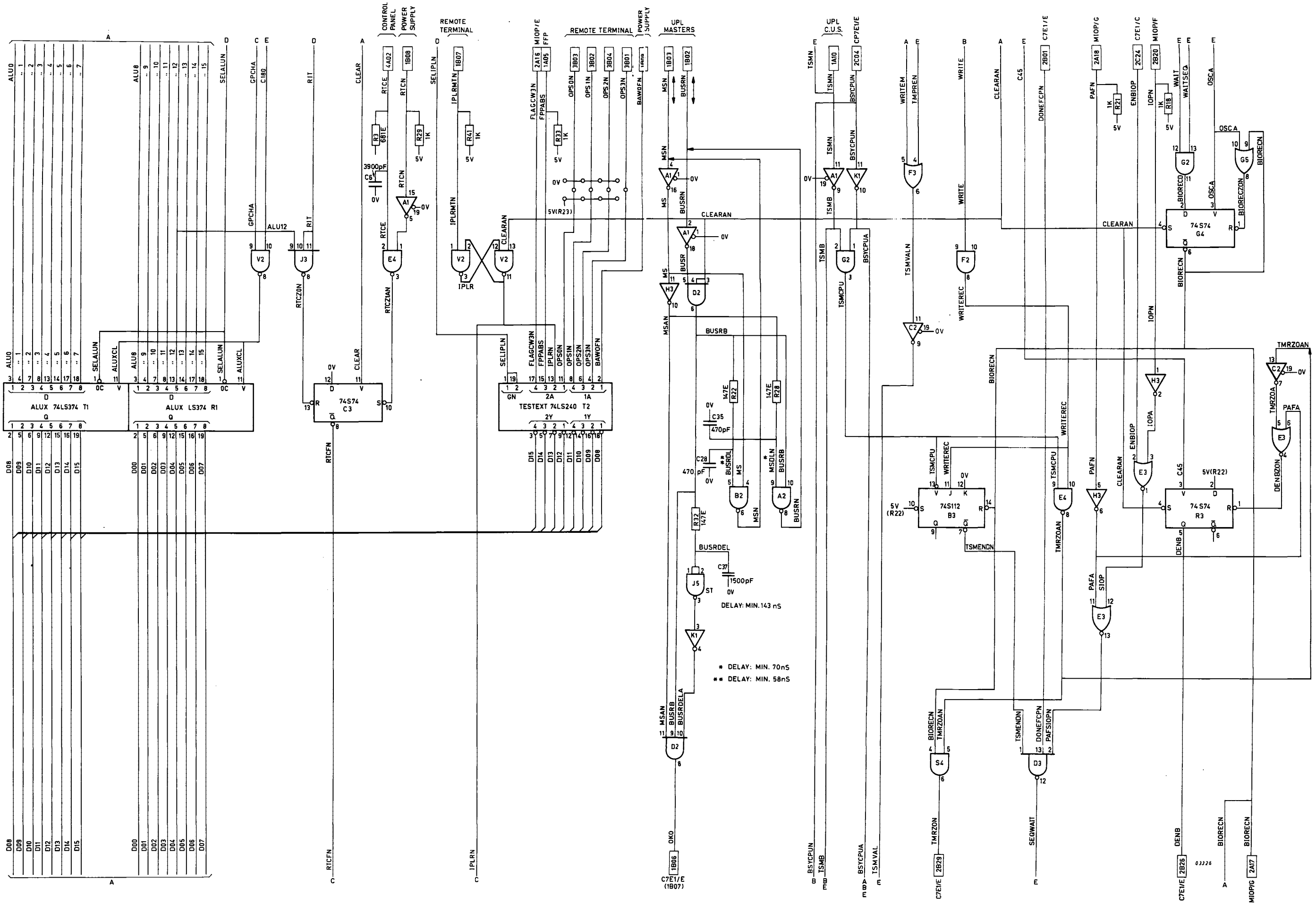
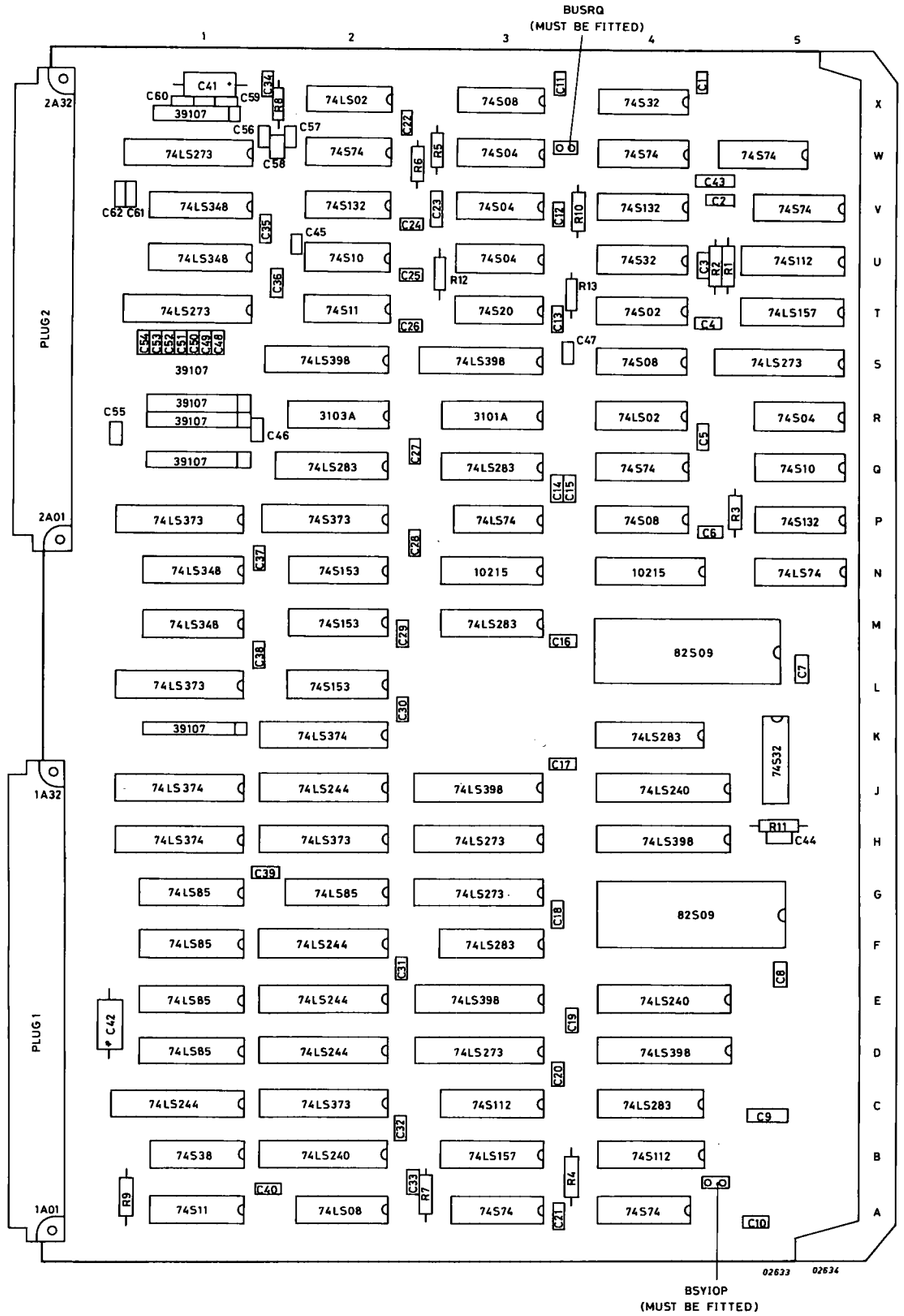


Figure 4.2F (C7E2A) ALUX, REMOTE IPL, BUS CONTROL LOGIC


BUSRQ
(MUST BE FITTED)
1
2
3
4
5
2A32
PLUG2
2A01
1A32
PLUG1
1A01
X
W
V
U
T
S
R
Q
P
N
M
L
K
J
H
G
F
E
D
C
B
A
C41
C60
C59
39107
C56
C57
C58
74LS02
74S08
74S32
74LS273
74S74
74S04
74S74
74S74
74LS348
74S132
74S04
74S132
74S74
74LS348
74S10
74S04
74S32
74S112
74LS273
74S11
74S20
74S02
74LS157
74LS398
74LS398
74S08
74LS273
39107
39107
3103A
3101A
74LS02
74S04
39107
74LS283
74LS283
74S74
74S10
74LS373
74S373
74LS74
74S08
74S132
74LS348
74S153
10215
10215
74LS74
74LS348
74S153
74LS283
82S09
74LS373
74S153
39107
74LS374
74LS283
74S32
74LS374
74LS244
74LS398
74LS240
74LS374
74LS373
74LS273
74LS398
74LS85
74LS85
74LS273
82S09
74LS85
74LS244
74LS283
74LS85
74LS244
74LS398
74LS240
74LS85
74LS244
74LS273
74LS398
74LS244
74LS373
74S112
74LS283
74S38
74LS240
74LS157
74S112
74S11
74LS08
74S74
74S74
C42
C39
C40
C44
C10
C9
C8
R1
R2
R3
R4
R5
R6
R7
R9
R10
R11
R12
R13
C1
C2
C3
C4
C5
C6
C7
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C35
C36
C37
C38
C43
C45
C46
C47
C48
C49
C50
C51
C52
C53
C54
02633
02634
BSYIOP
(MUST BE FITTED)

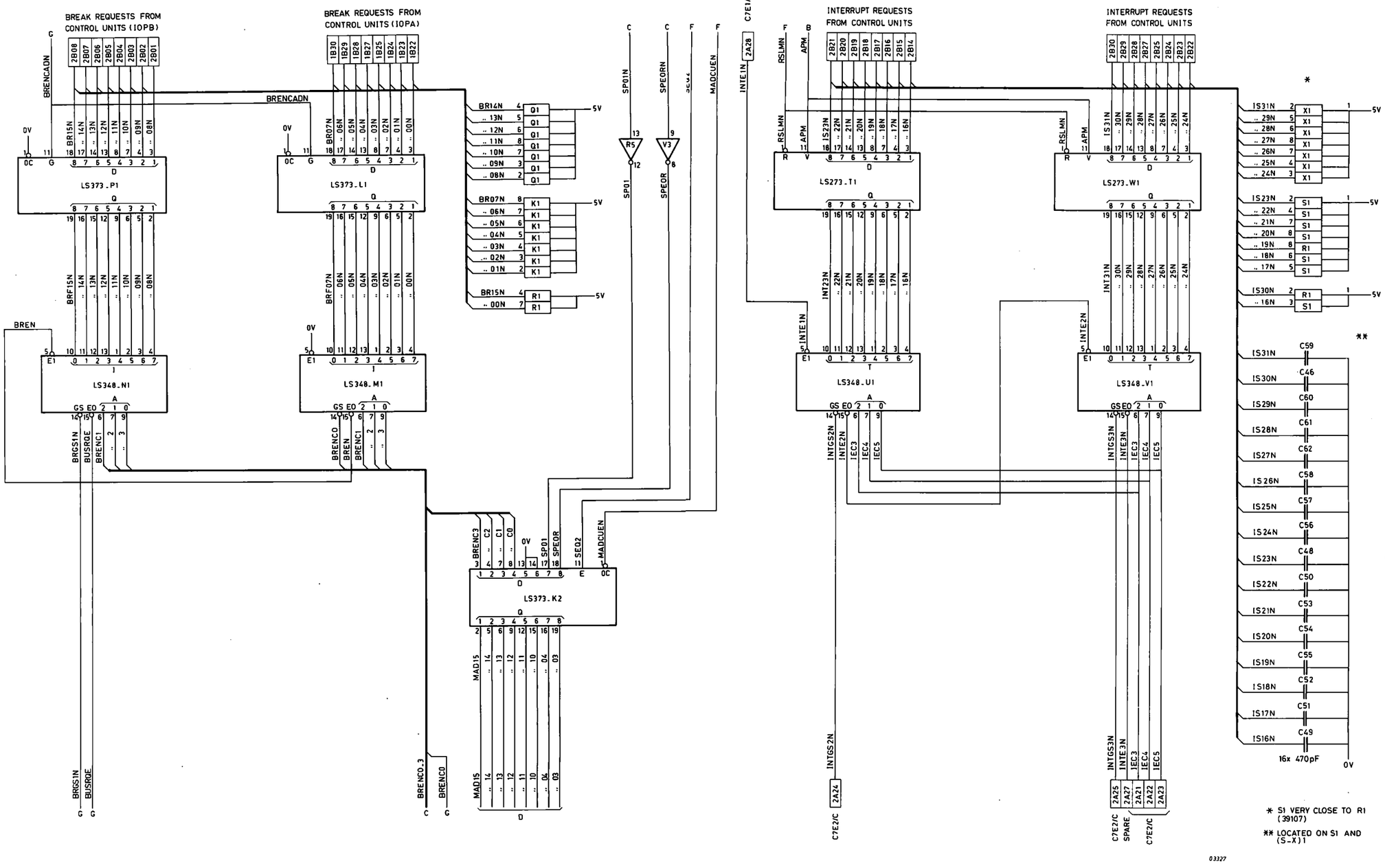


Figure 4.3A (MIOPB) BREAKS AND INTERRUPT ENCODING

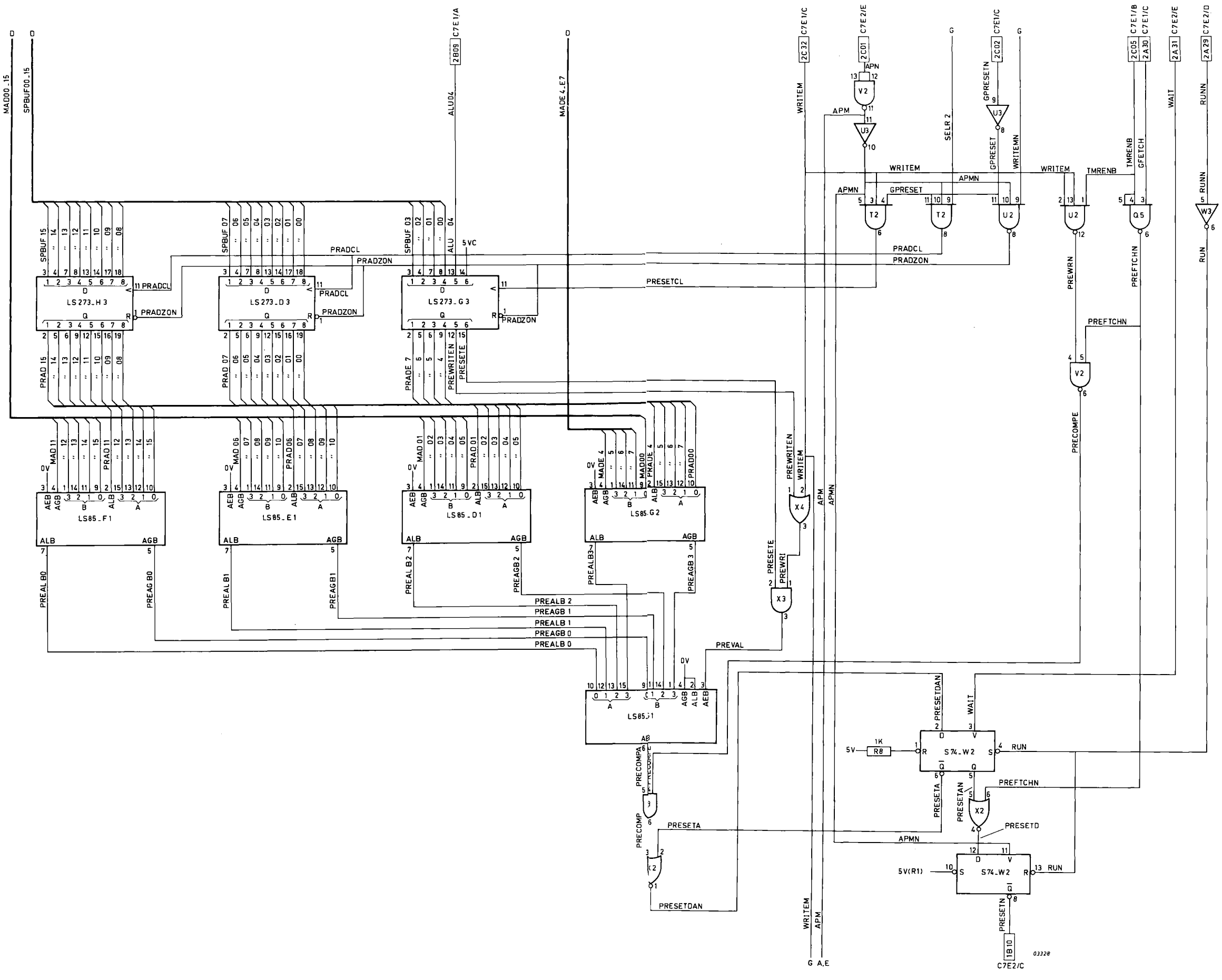


Figure 4.3B (MIOPB) STOP ON PRESET ADDRESS

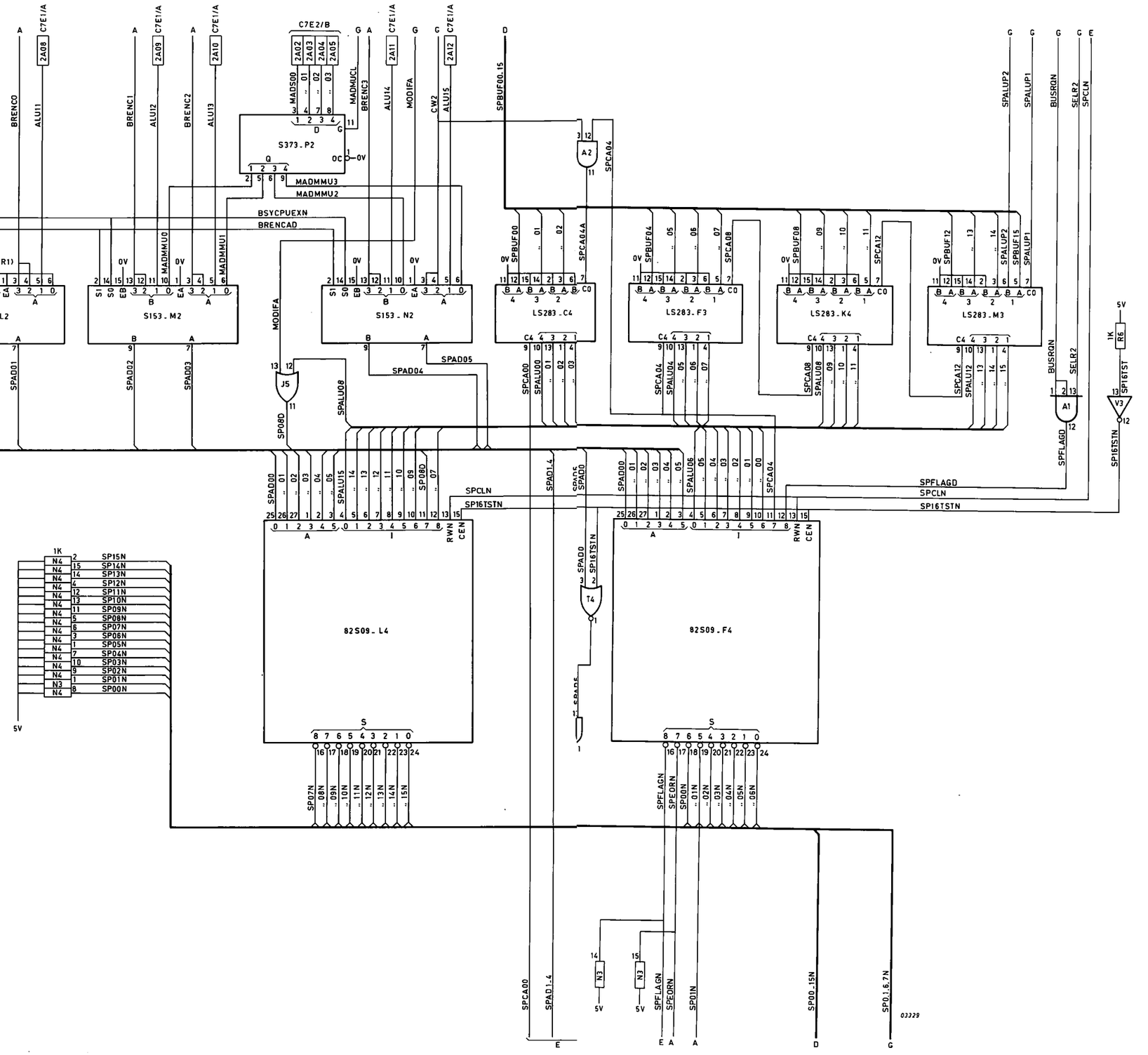


Figure 4.3C (MIOPB) SCRATCH PAD ADDRESSING

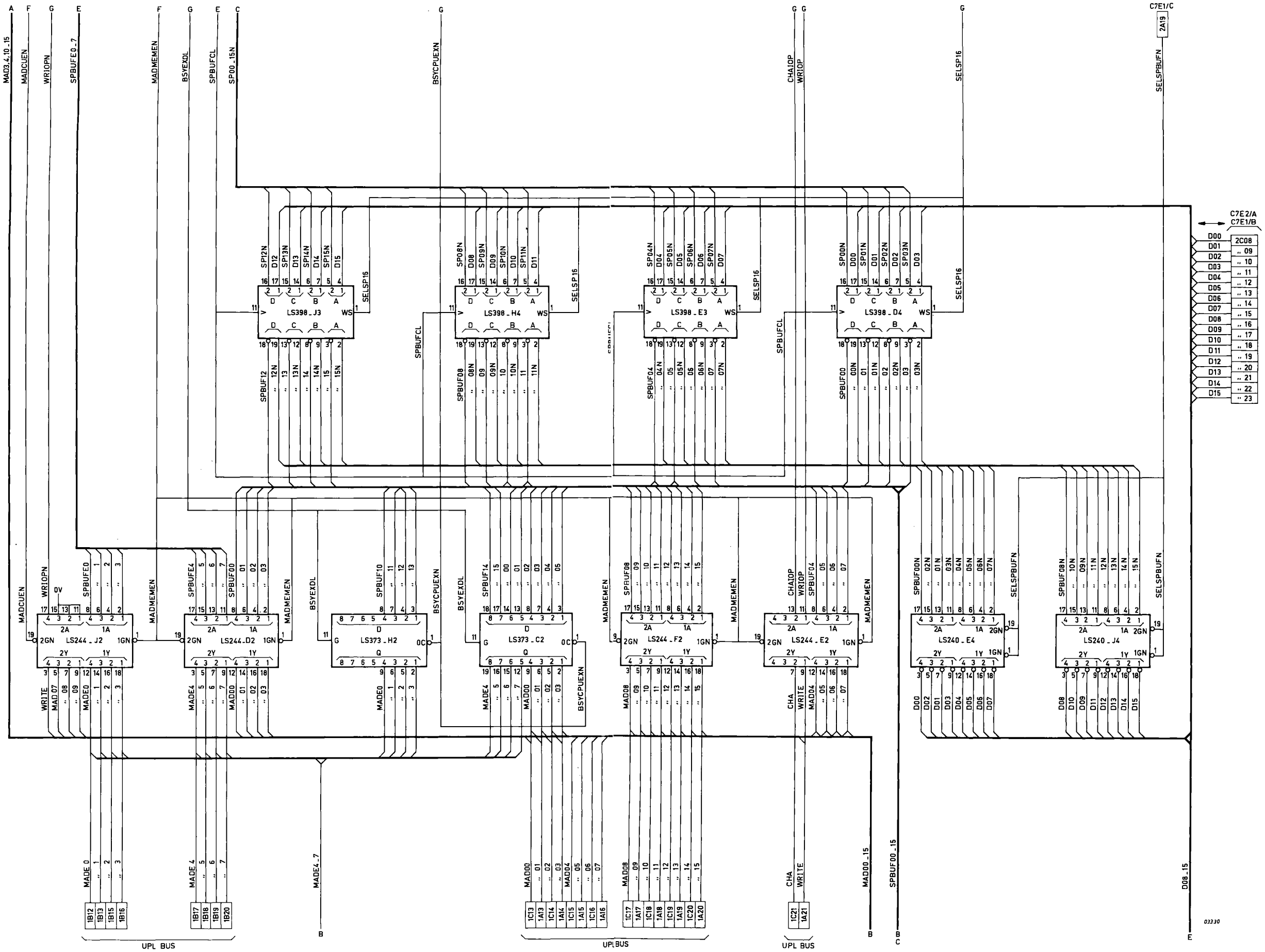


Figure 4.3D (MIOPA) SCRATCH PAD ADDRESSING

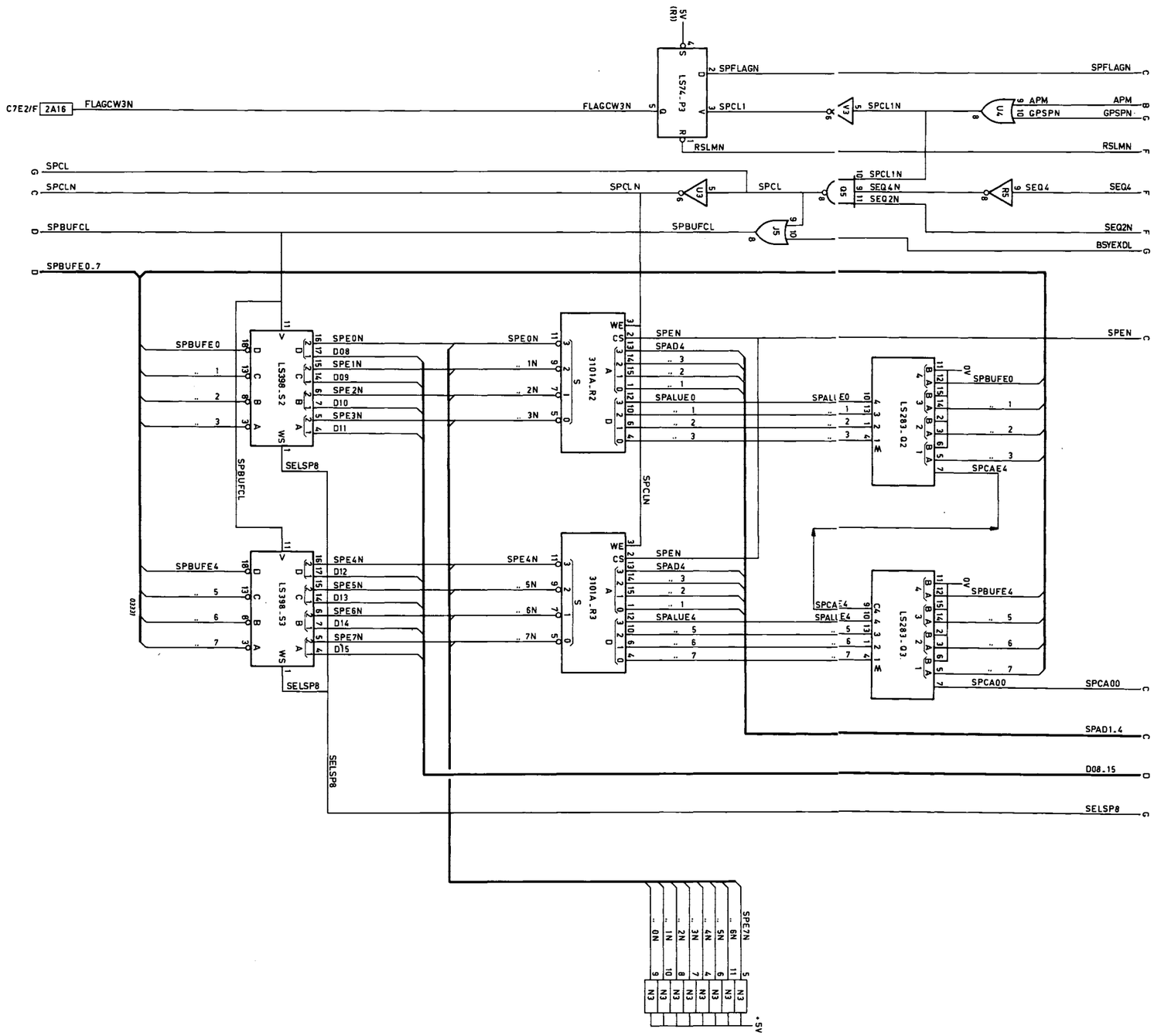


Figure 4.3E (MIOPB) SCRATCH PAD ADDRESSING

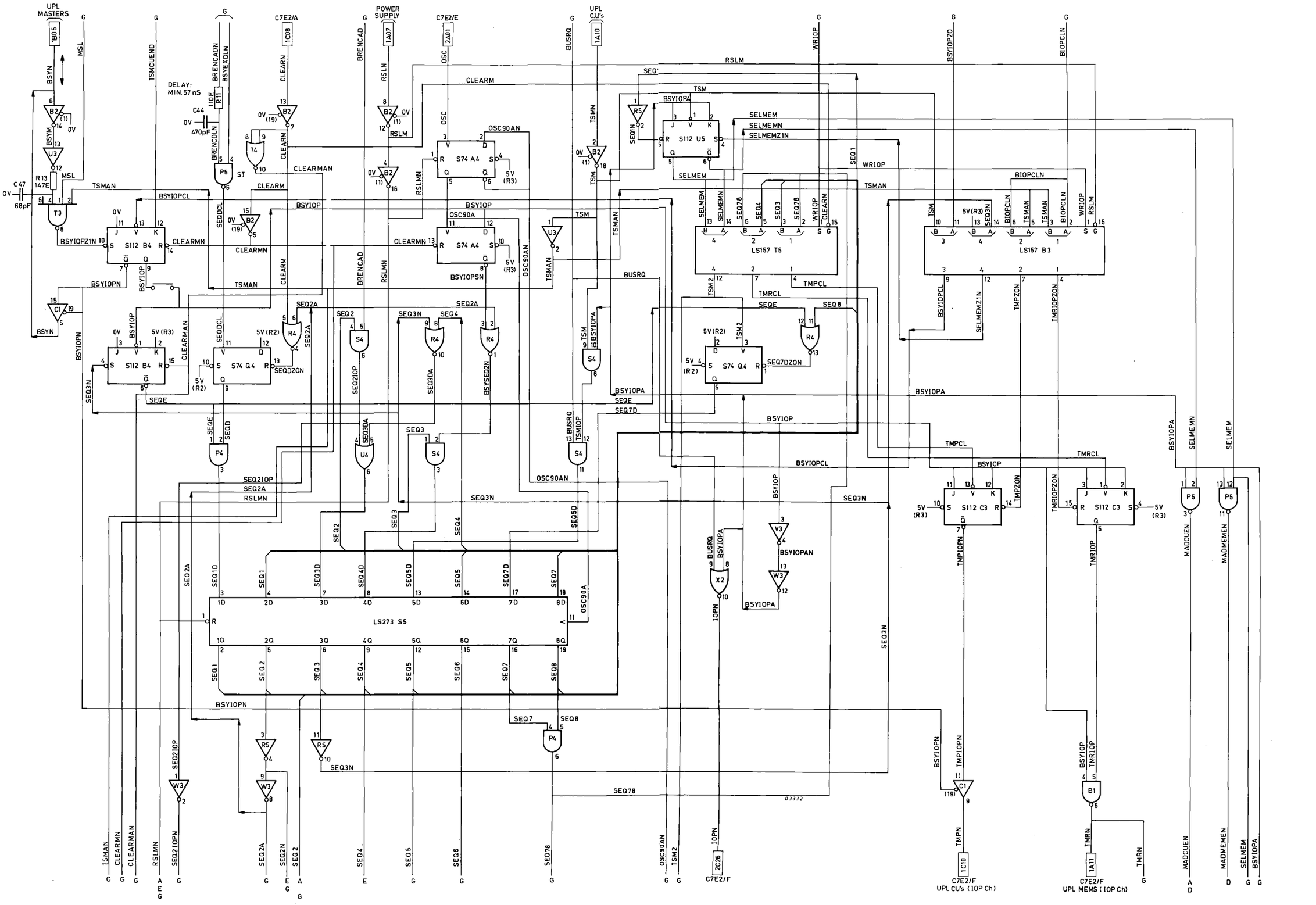


Figure 4.3F (MIOPB) SEQUENSOR

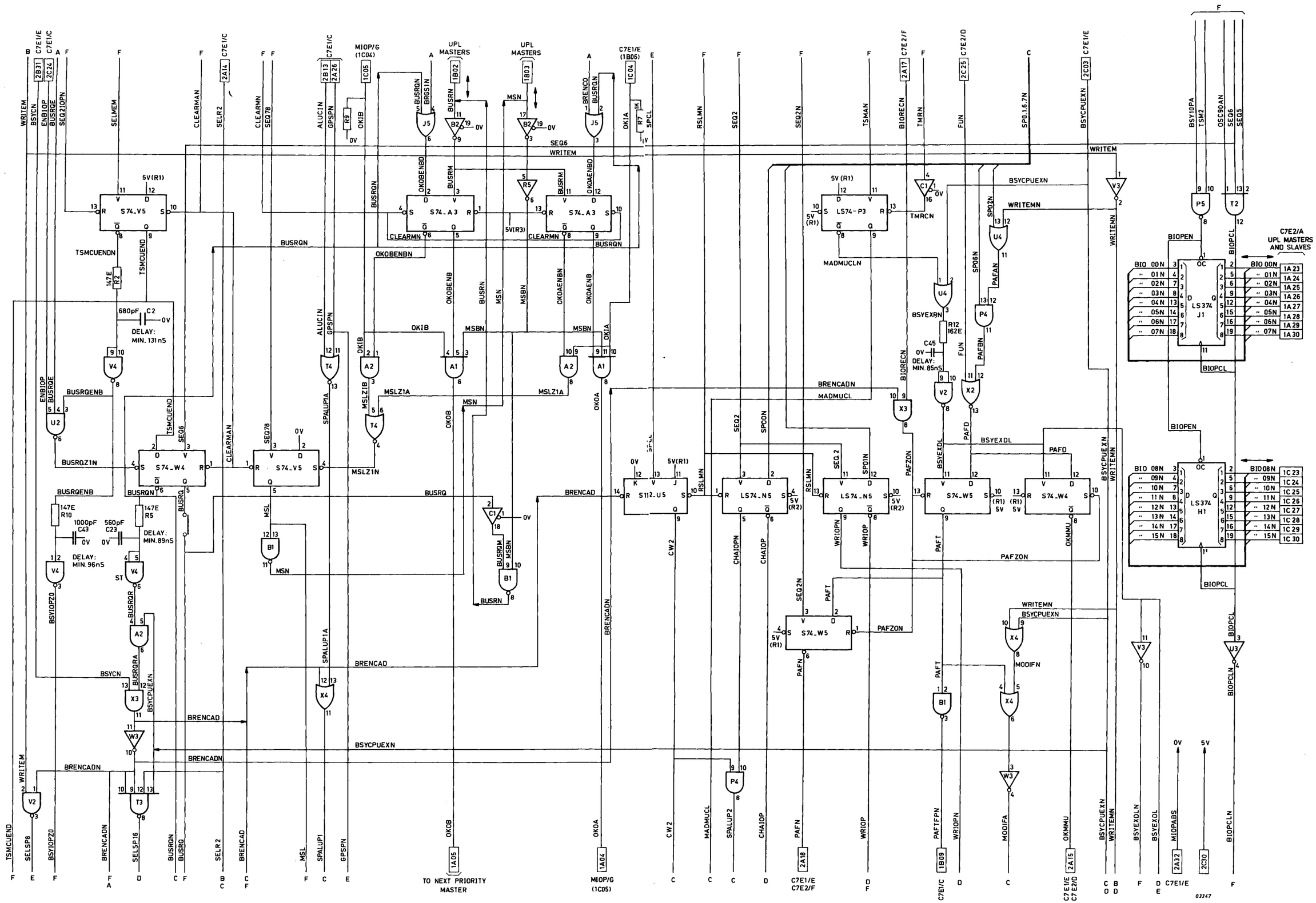
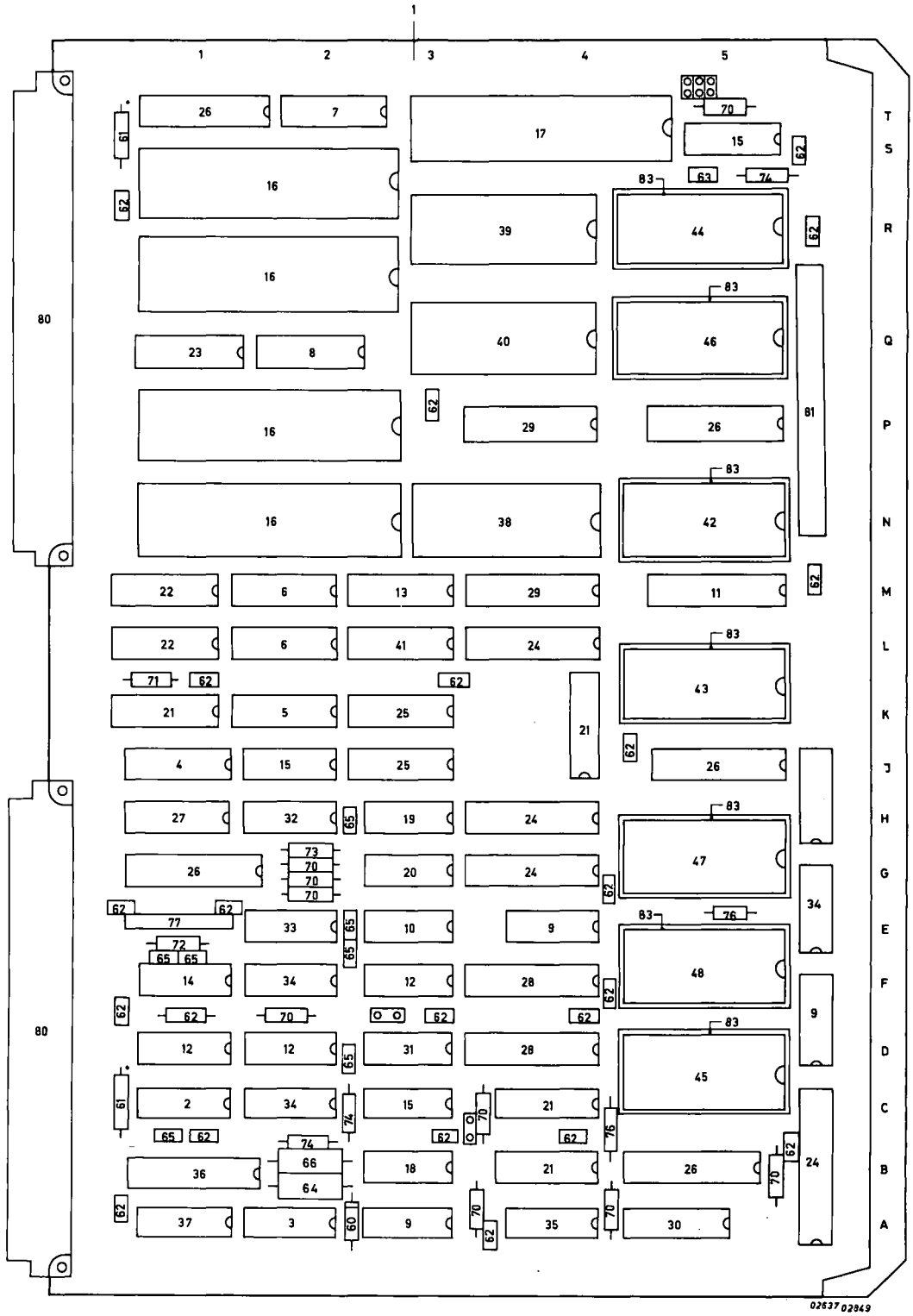


Figure 4.3G (MIOPA) BUS CONTROL LOGIC

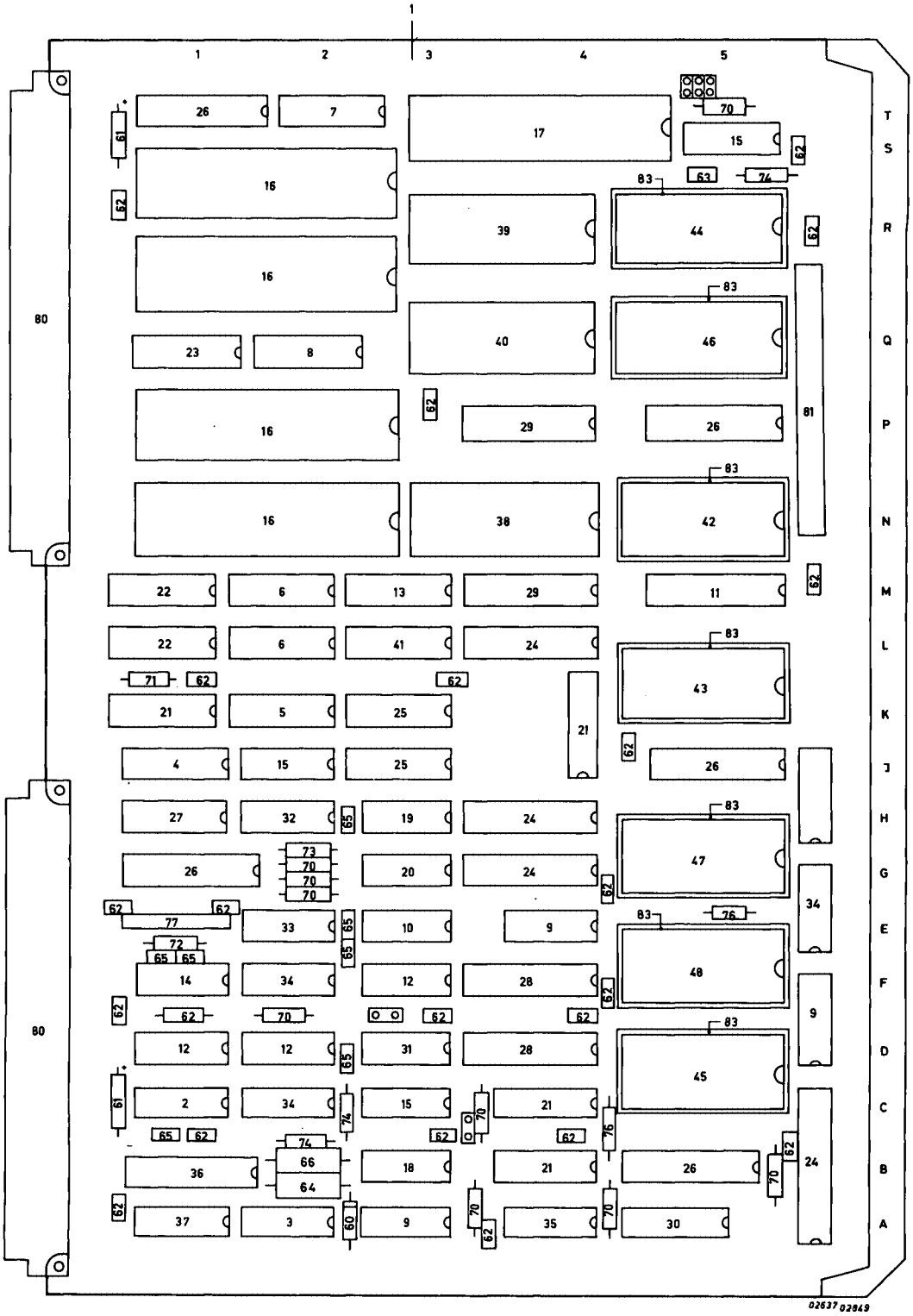
5 LISTING

Listings are not included in this document because of their limited usefullness, their bulk and related cost.
One copy of the listings will be made available to the LMO's upon receipt of a written request by an authorized official.

CARD LAYOUT C7E1-B

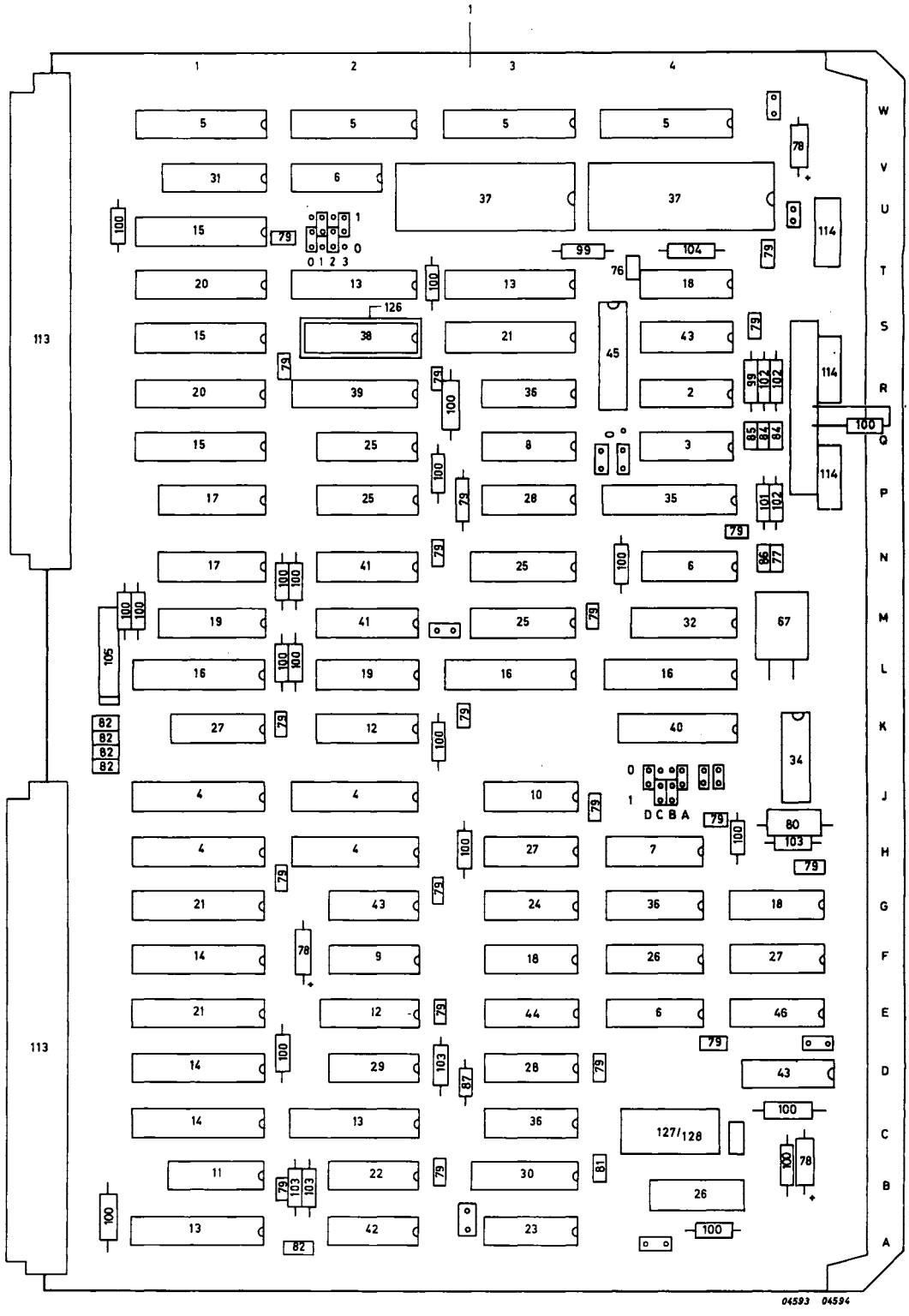


Pos.	Code Number	Description
A		P857EB
1B	5111 199 61980	PCB C7E1B Compl.
2C	5111 000 04291	IC 74S38
3C	5111 000 00921	IC 74S10
4C	5111 000 02531	IC 74S151
5C	5111 000 02301	IC 74S153
6C	5111 000 02451	IC 74S157
7C	5111 000 02151	IC 74S174
8C	5111 000 02541	IC 74S182
9C	5111 000 01791	IC 74S20
10C	5111 000 02721	IC 74S32
11C	5111 000 04121	IC 74S374
12C	5111 000 00791	IC 74S74
13C	5111 000 01821	IC 74S175
14C	5111 000 00801	IC 74S11
15C	5111 000 04071	IC 74S132
16C	5111 000 03742	IC 2901A
17C	5111 000 05401	IC 2910
18C	5111 000 02241	IC 74S02
19C	5111 000 02661	IC 74LS04
20C	5111 000 02701	IC 74LS08
21C	5111 000 02131	IC 74S138
22C	5111 000 04981	IC 74LS169
23C	5111 000 04131	IC 74LS173
24C	5111 000 04261	IC 74LS244
25C	5111 000 04051	IC 74LS251
26C	5111 000 03911	IC 74LS273
27C	5111 000 04021	IC 74LS348
28C	5111 000 03941	IC 74LS374
29C	5111 000 04011	IC 74LS377
30C	5111 000 03691	IC 74LS38
31C	5111 000 02831	IC 74LS74
32C	5111 000 02851	IC 74LS86
33C	5111 000 02241	IC 74S02
34C	5111 000 00491	IC 74S04
35C	5111 000 03891	IC 74S08
36C	5111 000 04091	IC 74LS240
37C	5111 000 00481	IC 74S00
38C	5111 010 04071	IC PLACR (82S100)
39C	5111 010 06741	IC PLAMAT (82S100)
40C	5111 010 06751	IC PLAVEC (82S100)
41C	5111 010 04101	IC PROM 4101 (82S123)
42C	5111 010 06483	IC 6483 (82S191) ROM 0
43C	5111 010 06493	IC 6493 (82S191) ROM 1
44C	5111 010 06503	IC 6503 (82S191) ROM 2
45C	5111 010 06513	IC 6513 (82S191) ROM 3
46C	5111 010 06523	IC 6523 (82S191) ROM 4
47C	5111 010 06534	IC 6534 (82S191) ROM 5
48C	5111 010 06544	IC 6544 (82S191) ROM 6


1
1
2
3
4
5
T
S
R
Q
P
N
M
L
K
J
H
G
E
F
D
C
B
A
80
80
81
26
7
17
70
61
15
62
16
63
74
83
39
44
16
40
46
23
8
29
26
16
38
42
22
6
13
29
11
22
6
41
24
71
43
21
5
25
21
4
15
25
26
27
32
19
24
47
26
20
24
34
77
33
10
9
72
48
14
34
12
28
9
12
12
31
28
45
2
34
15
21
74
66
64
36
18
21
26
24
37
3
9
35
30
60
02637 02849

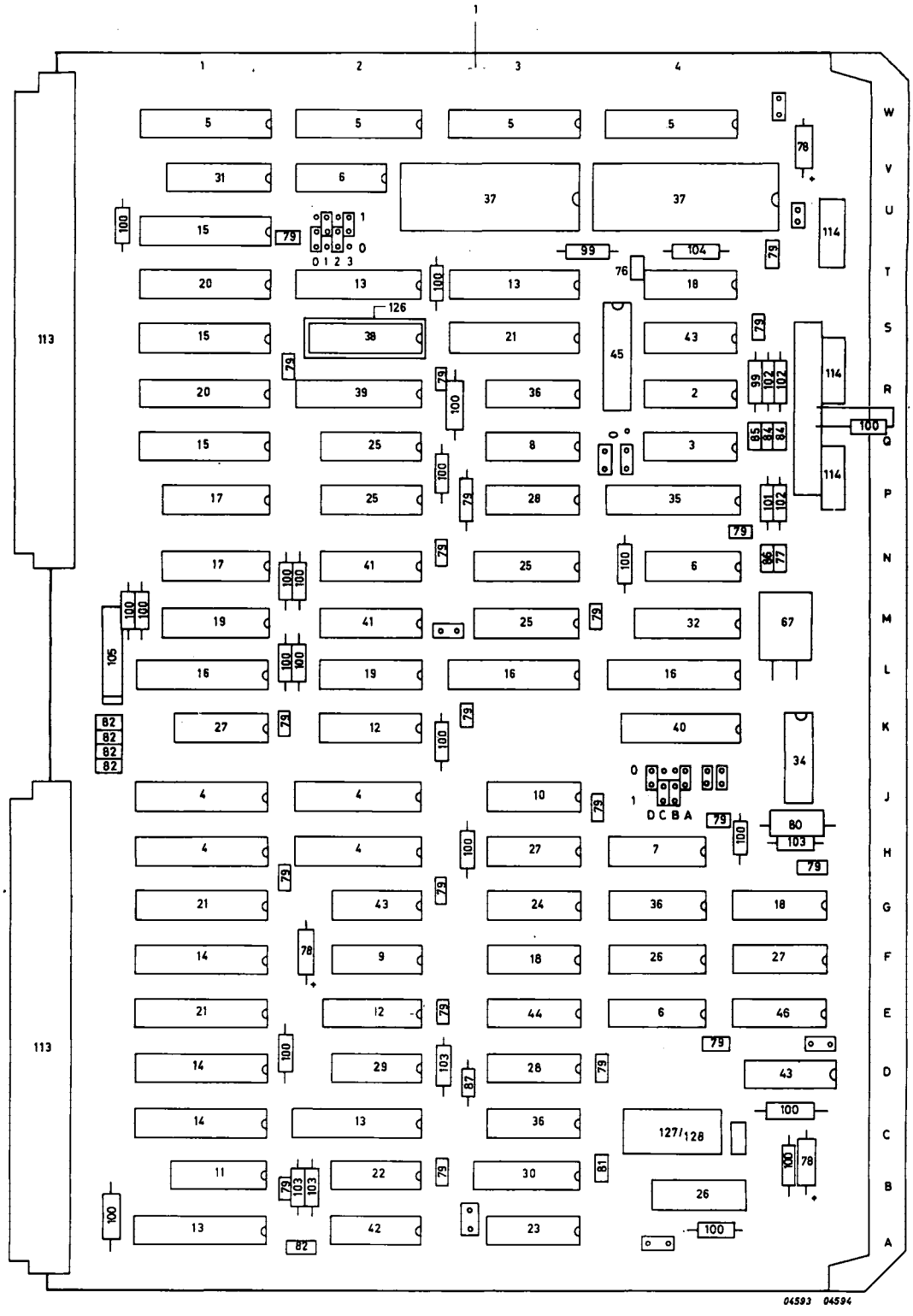
Pos.	Code Number	Description
60C	9331 126 70112	Diode 1N4151
61C	2222 030 38109	Capacitor 10uF 63V
62C	2222 629 18103	Capacitor 10nF 63V
63C	2222 630 18102	Capacitor 1000pF 10% 100V
64C	5111 000 07261	Capacitor 680pF 5%
65C	2222 630 18471	Capacitor 470pF 10% 100V
66C	5111 000 07271	Capacitor 820pF 5%
70C	2322 211 13102	Resistor 1K 5% 0.25W
71C	2322 211 13271	Resistor 270E 5% 0.25W
72C	2322 211 13391	Resistor 390E 5% 0.25W
73C	2311 211 13221	Resistor 220E 5% 0.25W
74C	2322 151 51471	Resistor 147E 1% 0 125W
75C	2322 211 13681	Resistor 680E 5% 0.25W
76C	2322 151 51101	Resistor 110E 1%
77C	5111 000 04241	Resistor network 39107
80C	5111 000 05711	Connector 8609 396 7113 245 000
81C	2422 025 02786	Connector 75789-101-40
83C	5111 000 05241	IC socket 24 pins

CARD LAYOUT C7E2-B



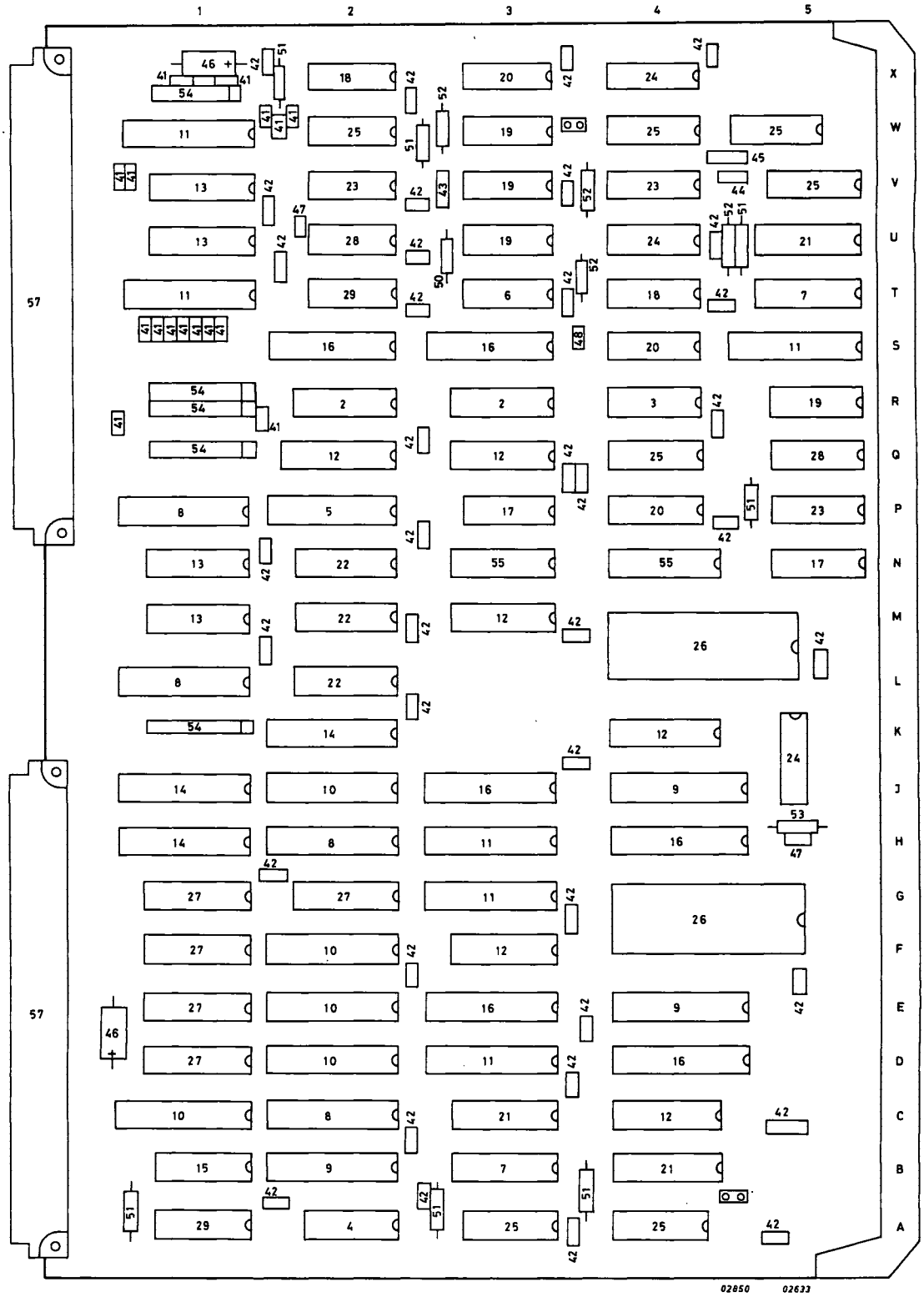
Pos.	Code Number	Description
A		P857EB
1B	5111 199 61990	PCB C7E2B Compl.
2C	5111 000 01871	IC 1488
3C	5111 000 01881	IC 1489A
4C	5111 000 04251	IC 2917
5C	9334 941 60682	IC AM 2932X
6C	5111 000 02651	IC 74LS00
7C	5111 000 02711	IC 74LS02
8C	5111 000 02661	IC 74LS04
9C	5111 000 02701	IC 74LS08
10C	5111 000 03641	IC 74LS10
11C	5111 000 02481	IC 74LS11
12C	5111 000 04981	IC 74LS169
13C	5111 000 04091	IC 74LS240
14C	5111 000 05361	IC 74LS373
15C	5111 000 04261	IC 74LS244
16C	5111 000 03911	IC 74LS273
17C	5111 000 02921	IC 74LS298
18C	5111 000 03671	IC 74S32
19C	5111 000 04021	IC 74LS348
20C	5111 000 03941	IC 74LS374
21C	5111 000 04011	IC 74LS377
22C	5111 000 03691	IC 74LS38
23C	5111 000 03871	IC 74LS393
24C	5111 000 02831	IC 74LS74
25C	5111 000 03591	IC 74LS85
26C	5111 000 00481	IC 74S00
27C	5111 000 00491	IC 74S04
28C	5111 000 00921	IC 74S10
29C	5111 000 00801	IC 74S11
30C	5111 000 00601	IC 74S112
31C	5111 000 02131	IC 74S138
32C	5111 000 02301	IC 74S153
33C	5111 000 03821	IC 74S20
34C	5111 000 04071	IC 74S132
35C	5111 000 04121	IC 74S374
36C	5111 000 00791	IC 74S74
37C	5111 000 04271	IC 8251A
38C	5111 000 04601	IC PROM 4601 (82S137)
39C	5111 000 04371	IC 8304B
40C	9336 520 20682	IC COM8116
41C	5111 000 02691	IC 74LS157
42C	5111 000 04291	IC 74S38
43C	5111 000 03891	IC 74S08
44C	5111 000 02241	IC 74S02
45C	5111 000 03801	IC 74LS123
46C	5111 000 07081	IC 74F74
67C	2411 535 01332	Crystal QA60A 5,0688 MHZ

CARD LAYOUT C7E2-B



Pos.	Code Number	Description
76C	5111 000 06711	Capacitor 1uF 50V
77C	2222 630 01102	Capacitor 1000pF 10% 100V
78C	2222 015 28109	Capacitor 10uF 25V
79C	2222 629 18103	Capacitor 10nF CER
80C	2222 424 41502	Capacitor 1500pF 1% 63V
81C	2222 630 18472	Capacitor 4,7nF 10%
82C	2222 630 01471	Capacitor 470pF
84C	2222 630 18391	Capacitor 390pF
85C	2222 630 18392	Capacitor 3900pF
86C	2013 553 00561	Capacitor 0,1uF 50V
87C	2222 427 44701	Capacitor 470pF 1%
99C	2322 151 56811	Resistor 681E
100C	2322 211 13102	Resistor 1K 5% 0,25W
101C	2322 151 56812	Resistor 6,81K 1% 0,125W
102C	2322 211 13221	Resistor 220E 5% 0,25W
103C	2322 151 51471	Resistor 147E 1% 0,125W
104C	2322 151 52614	Resistor 261K 1% 0,125W
105C	5111 000 04241	Resistor network 39107
113C	5111 000 05711	Connector 8609 396 7112 245 000
114C	2422 000 02281	Connector 75789 - 101 -10
126C	5111 000 05221	IC socket 16 pins
127C	5111 000 07161	IC LOCO K1100A-22,220 MHz
128C	5122 110 91491	Insulation Plate (under LOCO)

CARD LAYOUT MIOP-B



Pos.	Code Number	Description
A		P857EB
1B	5111 199 62000	PCB MIOPB COMPL.
2C	5111 000 00941	IC 3101A
3C	5111 000 02711	IC 74LS02
4C	5111 000 02701	IC 74LS08
5C	5111 000 04111	IC 74S373
6C	5111 000 02241	IC 74S20
7C	5111 000 02691	IC 74LS157
8C	5111 000 05361	IC 74LS373
9C	5111 000 04091	IC 74LS240
10C	5111 000 04261	IC 74LS244
11C	5111 000 03911	IC 74LS273
12C	5111 000 02911	IC 74LS283
13C	5111 000 04021	IC 74LS348
14C	5111 000 03941	IC 74LS374
15C	5111 000 04291	IC 74S38
16C	5111 000 05371	IC 74LS398
17C	5111 000 02831	IC 74LS74
18C	5111 000 02241	IC 74S02
19C	5111 000 00491	IC 74S04
20C	5111 000 03891	IC 74S08
21C	5111 000 00601	IC 74S112
22C	5111 000 02301	IC 74S153
23C	5111 000 04071	IC 74S132
24C	5111 000 03671	IC 74S32
25C	5111 000 00791	IC 74S74
26C	5111 000 03961	IC 82S09
27C	5111 000 03591	IC 74LS85
28C	5111 000 00921	IC 74S10
29C	5111 000 00801	IC 74S11
41C	2222 630 18471	Capacitor 470pF
42C	2222 629 18103	Capacitor 10nF
43C	2013 554 18401	Capacitor 560pF 1% 100V
44C	2013 554 08352	Capacitor 680pF 5% 100V
45C	2013 554 08353	Capacitor 1000pF 5% 100V
46C	2222 015 28109	Elco 10uF 25V
47C	2013 554 08403	Capacitor 470pF 1% 100V
48C	2222 631 10689	Capacitor 68pF
50C	2322 151 51621	Resistor 162E 0,125W 1%
51C	2322 211 13102	Resistor 1K 0, 25W 5%
52C	2322 151 51471	Resistor 147E 1,125W 1%
53C	2322 151 51101	Resistor 110E 0,125W 1%
54C	5111 000 04241	Resistor network 39107
55C	5111 000 03931	Resistor network 10215
57C	5111 000 05711	Connector 8609 396 7113 245000

ARTNR:	S12NC:	DESCR
2222 015 28109	4822 124 20728	ELCO 10MU 63V
2222 030 38109	4822 124 20728	CAP. 10UF 63V
2222 629 01103	4822 122 30043	CAP. 10NF 10% 63V
2222 629 18103	4822 122 30043	CAP. 10NF 63V
2222 630 01102	4822 122 30027	CAP.1000PF 100V 10%
2222 630 01471	4822 122 30034	CAP.470PF 10% 100V
2222 630 18102	4822 122 30027	CAP 1000PF 10% 100V
2222 630 18471	4822 122 30034	CAP 470PF 10% 100V
2322 151 51101	5322 116 54474	RES.110E 1% 1/8W
2322 151 51471	5322 116 50766	RES.147E 1% 1/8W
2322 211 13102	4822 110 73107	RES. 1KO 5% 0.25W
2322 211 13221	4822 110 73089	RES.220E 5% 0.25W
2322 211 13271	4822 110 73092	RES.270E 5% 0.25W
2322 211 13391	4822 110 73096	RES.390E 5% 0.25W
2322 211 13681	4822 110 73103	RES.680E 5% 0.25W
2411 024 01024	5322 268 10182	JUMPER LINK 2MM54
2422 025 02786	5322 265 64122	CONN.725789-101-40
5111 000 00481	5322 209 84167	IC SN74S00N
5111 000 00491	5322 209 84475	IC N74S04A
5111 000 00791	5322 209 84183	IC SN74S74N
5111 000 00801	5322 209 85604	IC N74S11N
5111 000 00921	5322 209 84954	IC SN74S10N
5111 000 01791	5322 209 85195	IC SN74S20N
5111 000 01821	5322 209 85451	IC N74S175B
5111 000 02131	5322 209 86439	IC N74S138B
5111 000 02151	5322 209 85683	IC N74S174B
5111 000 02241	5322 209 85407	IC N74S02A
5111 000 02301	5322 209 85688	IC N74S153B
5111 000 02451	5322 209 85669	IC SN74S157N
5111 000 02531	5322 209 85453	IC N74S151B
5111 000 02541	5322 209 85814	IC N74S182F
5111 000 02661	4822 209 80783	IC 74LS04
5111 000 02701	5322 209 84995	IC SN74LS08N
5111 000 02831	4822 209 80782	IC 74LS74A
5111 000 02851	5322 209 84997	IC SN74LS86N
5111 000 03671	5322 209 85679	IC N74S32A
5111 000 03742	5322 209 85817	IC AM2901ADC
5111 000 03891	5322 209 85681	IC N74S08A
5111 000 03911	5322 209 85792	IC N74LS273N
5111 000 03941	5322 209 85869	IC SN74LS374N
5111 000 04011	5322 209 86258	IC 74LS377
5111 000 04021	5322 209 86259	IC 74LS348
5111 000 04051	5322 209 86224	IC SN74LS251
5111 000 04071	5322 209 85267	IC SN74S132N
5111 000 04091	5322 209 85862	IC SN74LS240N
5111 000 04121	5322 209 86162	IC 74S374
5111 000 04131	5322 209 85967	IC N74LS173N
5111 000 04241	5322 111 94221	R.NETW.39107(7X390E)
5111 000 04261	5322 209 86017	IC N74LS244N
5111 000 04291	5322 209 85677	IC 74S38
5111 000 04981	5322 209 86393	IC 74LS169
5111 000 05241	5322 255 44229	SOCKET 24POL. (DIL)
5111 000 05401	5322 209 86395	IC AM2910DC
5111 000 07261	5322 121 50878	CAP 680PF 250V 5%
5111 000 07271	5322 121 54072	CAP 820PF 250V 5%
9331 126 70112	5322 130 34321	DIODE 1N4151

ARTNR:	S12NC:	DESCR
2222 030 28109	4822 124 20728	CAP 10UF
2222 629 18103	4822 122 30043	CAP. 10NF 100V
2222 630 18102	4822 122 30027	KER-CAP 1N 63V
2222 630 18391	4822 122 30091	CAP 390PF
2222 630 18392	4822 122 30098	CAP.3900PF
2222 630 18471	4822 122 30034	CAP 470PF 10% 100V
2222 630 18472	4822 122 30128	CAP 4700PF
2322 151 51471	5322 116 50766	RES.147E 1% 1/8W
2322 151 52614	5322 116 54736	RES.261K 1% 1/8W
2322 151 56811	4822 116 51233	RES.681E 1% 1/8W
2322 151 56812	4822 116 51252	RES.6K81 1/8W 1%
2322 211 13102	4822 110 73107	RES. 1KO 5% 0.25W
2322 211 13221	4822 110 73089	RES.220E 5% 0.25W
2411 011 07257	5322 268 14116	PIN QW786
2411 024 01024	5322 268 10182	JUMPER LINK 2MM54
2411 535 01332	5322 242 74147	CRYSTAL 5,0688MHZ
2422 025 02281	5322 265 44121	CONN. 75789-101-10
5111 000 00481	5322 209 84167	IC SN74S00N
5111 000 00491	5322 209 84475	IC N74S04A
5111 000 00601	5322 209 85741	IC SN74S112N
5111 000 00791	5322 209 84183	IC SN74S74N
5111 000 00801	5322 209 85604	IC N74S11N
5111 000 00921	5322 209 84954	IC SN74S10N
5111 000 01871	5322 209 84307	IC SN75188
5111 000 01881	5322 209 85619	IC 1489A
5111 000 02131	5322 209 86439	IC N74S138B
5111 000 02241	5322 209 85407	IC N74S02A
5111 000 02301	5322 209 85688	IC N74S153B
5111 000 02481	5322 209 85604	IC N74LS11A
5111 000 02651	5322 209 84823	IC N74LS00A
5111 000 02661	4822 209 80783	IC 74LS04
5111 000 02691	5322 209 85489	IC N74LS157B
5111 000 02701	5322 209 84995	IC SN74LS08N
5111 000 02711	5322 209 85312	IC N74LS02A
5111 000 02831	4822 209 80782	IC 74LS74A
5111 000 02921	5322 209 85937	IC N74LS298N
5111 000 03591	5322 209 85615	IC N74LS85N
5111 000 03641	5322 209 84996	IC N74LS10A
5111 000 03671	5322 209 85679	IC N74S32A
5111 000 03691	5322 209 85605	IC N74LS38A
5111 000 03801	5322 209 85266	IC SN74LS123N
5111 000 03871	4822 209 80447	IC N74LS393N
5111 000 03891	5322 209 85681	IC N74S08A
5111 000 03911	5322 209 85792	IC N74LS273N
5111 000 03941	5322 209 85869	IC SN74LS374N
5111 000 04011	5322 209 86258	IC 74LS377
5111 000 04021	5322 209 86259	IC 74LS348
5111 000 04071	5322 209 85267	IC SN74S132N
5111 000 04091	5322 209 85862	IC SN74LS240N
5111 000 04121	5322 209 86162	IC 74S374
5111 000 04241	5322 111 94221	R.NETW.39107(7X390E)
5111 000 04251	5322 209 86246	IC 2917A
5111 000 04261	5322 209 86017	IC N74LS244N
5111 000 04271	5322 209 85847	IC P8251A
5111 000 04291	5322 209 85677	IC 74S38

PCB C7E2-B

ARTNR:	S12NC:	DESCR
5111 000 04371	5322 209 86211	IC 8304D
5111 000 04981	5322 209 86393	IC 74LS169
5111 000 05361	4822 209 80916	IC SN74LS373J
5111 000 06711	4822 124 20927	CAP 1UF 50V
5111 000 07081	5322 209 81474	IC 74F74PC
5111 000 07161	5322 242 70644	X-TAL 22,220MHZ
5111 000 07231	5322 122 31911	CAP BT 5% 470PF
5111 000 07301	5322 121 50913	CAP BT 5% 1NF5
5111 000 07831	5322 122 31951	CAP 0UF1 50V
9334 941 60682	5322 209 86396	IC AM2932DC
9336 520 20682	5322 209 81547	IC COM8116P

PCB MIOP-B

ARTNR:	S12NC:	DESCR
2013 554 08351	5322 122 31703	CAP 470PF 1% 100V
2013 554 08352	5322 122 31699	CAP 680PF 5% 100V
2013 554 08353	5322 122 31701	CAP 1000PF 5% 100V
2013 554 08401	5322 122 31702	CAP 560PF 1% 100V
2222 015 16109	4822 124 20697	CAP.10UF 25V
2222 629 01103	4822 122 30043	CAP. 10NF 10% 63V
2222 630 01471	4822 122 30034	CAP.470PF 10% 100V
2222 631 10689	4822 122 31076	CAP..68PF 2% 100V
2322 151 51101	5322 116 54474	RES.110E 1% 1/8W
2322 151 51471	5322 116 50766	RES.147E 1% 1/8W
2322 151 51621	5322 116 50417	RES.162E 1% 1/8W
2322 211 13102	4822 110 73107	RES. 1KO 5% 0.25W
2411 024 01024	5322 268 10182	JUMPER LINK 2MM54
5111 000 00491	5322 209 84475	IC N74S04A
5111 000 00601	5322 209 85741	IC SN74S112N
5111 000 00791	5322 209 84183	IC SN74S74N
5111 000 00801	5322 209 85604	IC N74S11N
5111 000 00921	5322 209 84954	IC SN74S10N
5111 000 00941	5322 209 54058	ROM 3101A
5111 000 01791	5322 209 85195	IC SN74S20N
5111 000 02241	5322 209 85407	IC N74S02A
5111 000 02301	5322 209 85688	IC N74S153B
5111 000 02691	5322 209 85489	IC N74LS157B
5111 000 02701	5322 209 84995	IC SN74LS08N
5111 000 02711	5322 209 85312	IC N74LS02A
5111 000 02831	4822 209 80782	IC 74LS74
5111 000 02911	5322 209 86052	IC 74LS283
5111 000 03591	5322 209 85615	IC N74LS85N
5111 000 03671	5322 209 85679	IC N74S32A
5111 000 03891	5322 209 85681	IC N74S08A
5111 000 03911	5322 209 85792	IC N74LS273N
5111 000 03931	5322 111 94237	RNW 10215(15X1K)
5111 000 03941	5322 209 85869	IC SN74LS374N
5111 000 03961	5322 209 54526	IC 82S09
5111 000 04021	5322 209 86259	IC 74LS348
5111 000 04071	5322 209 85267	IC SN74S132N
5111 000 04091	5322 209 85862	IC SN74LS240N
5111 000 04111	5322 209 86086	IC 74S373
5111 000 04241	5322 111 94221	R.NETW.39107(7X390E)
5111 000 04261	5322 209 86017	IC N74LS244N
5111 000 04291	5322 209 85677	IC 74S38
5111 000 05361	4822 209 80916	IC SN74LS373J
5111 000 05371	5322 209 86394	SOCKET 28POL. (DIL)